MODULE 1

SEMICONDUCTOR DIODE and It's APPLICATIONS

Presented By:

GOUTHAM V
Asst. Prof. Dept. of ECE
BGSIT, B G Nagar

Diode

A diode is a semiconductor device which eases conduction in one direction and stops conduction in other direction. It has two terminals namely Anode and Cathode.

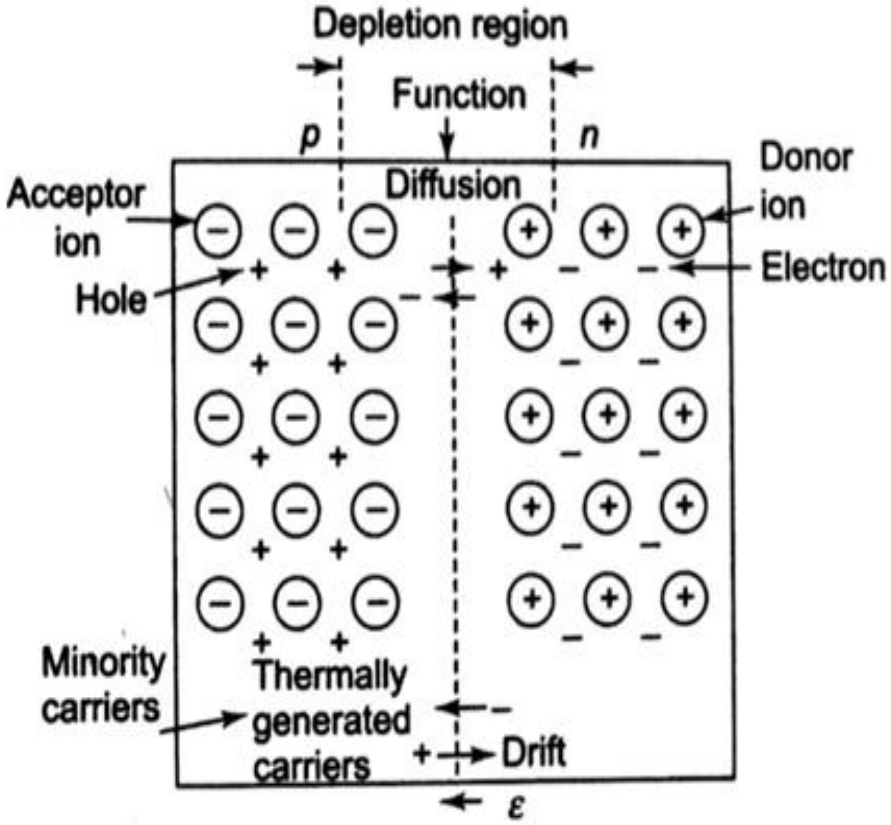
It has wide range of applications like;

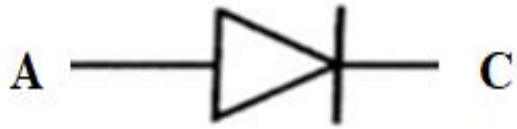
- Rectification
- Voltage Regulation
- Wave Shaping etc.

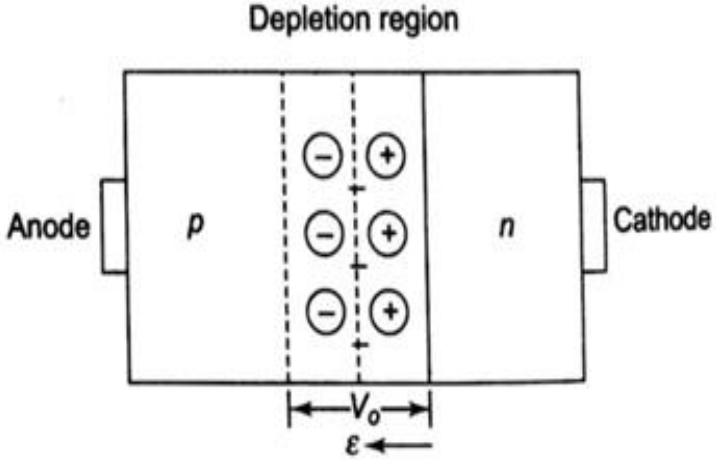
PN- Junction Diode

Construction:

- When a thin layer of P-type semiconductor and N-type semiconductor are placed together, a junction in formed called as PN junction.
- The P-side is called Anode [A] and the N-side is called Cathode [C].
- Majority holes from P-side diffuses (moves) to N-side and Majority electrons from N-side diffuses (moves) to P-side.
- Recombination of holes and electrons forms a narrow region on both side of the junction which forms fixed positive ions at N-side and negative ions at P-side.
- This region is called ***Depletion Region*** where no free electrons and holes are present.
- At the junction an electric field is created which opposes the flow of charges.
- In steady state, there is no net current flow across junction.


Depletion region
Function
p
n
Diffusion
Acceptor ion
Donor ion
Hole
Electron
Minority carriers
Thermally generated carriers
Drift
ε

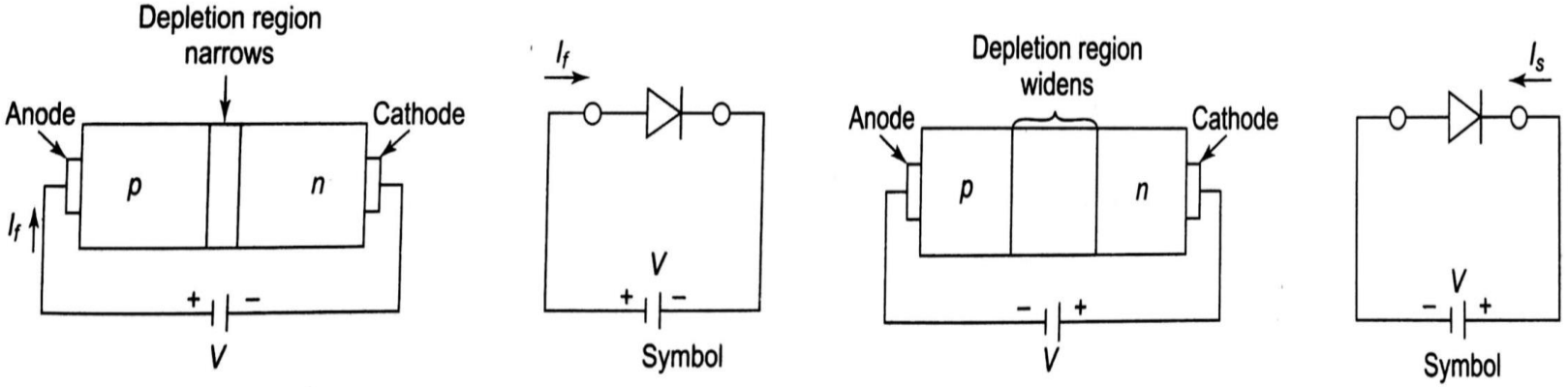

A
C


Depletion region
Anode
p
n
Cathode
V_o
ε

Biasing:

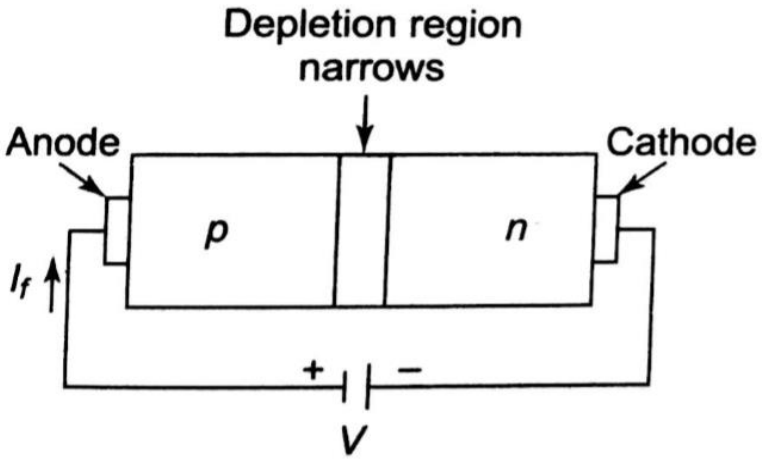
Applying an external voltage to a device is called Biasing. There are two types of biasing;

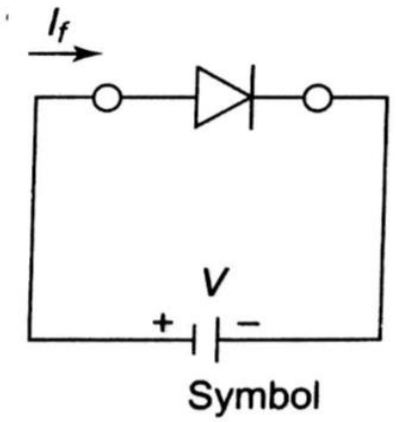
- Forward Biasing
- Reverse Biasing



Forward Biasing

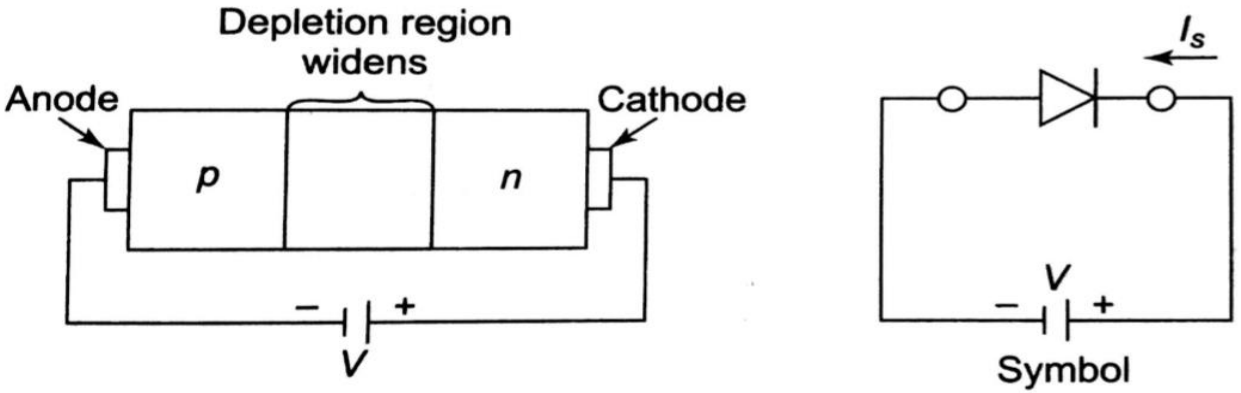
- When the positive terminal of the battery is connected to the Anode (P-side) and negative terminal is connected to the Cathode (N-side), diode is said to be forward biased.
- The holes from P-type and electrons from N-type are moved towards the junction, reducing the depletion region.
- Hence, holes moves towards N-side and electrons moves towards P-side easily which produces the Current in the diode $\mathbf{I_d}$ (Diode Current)

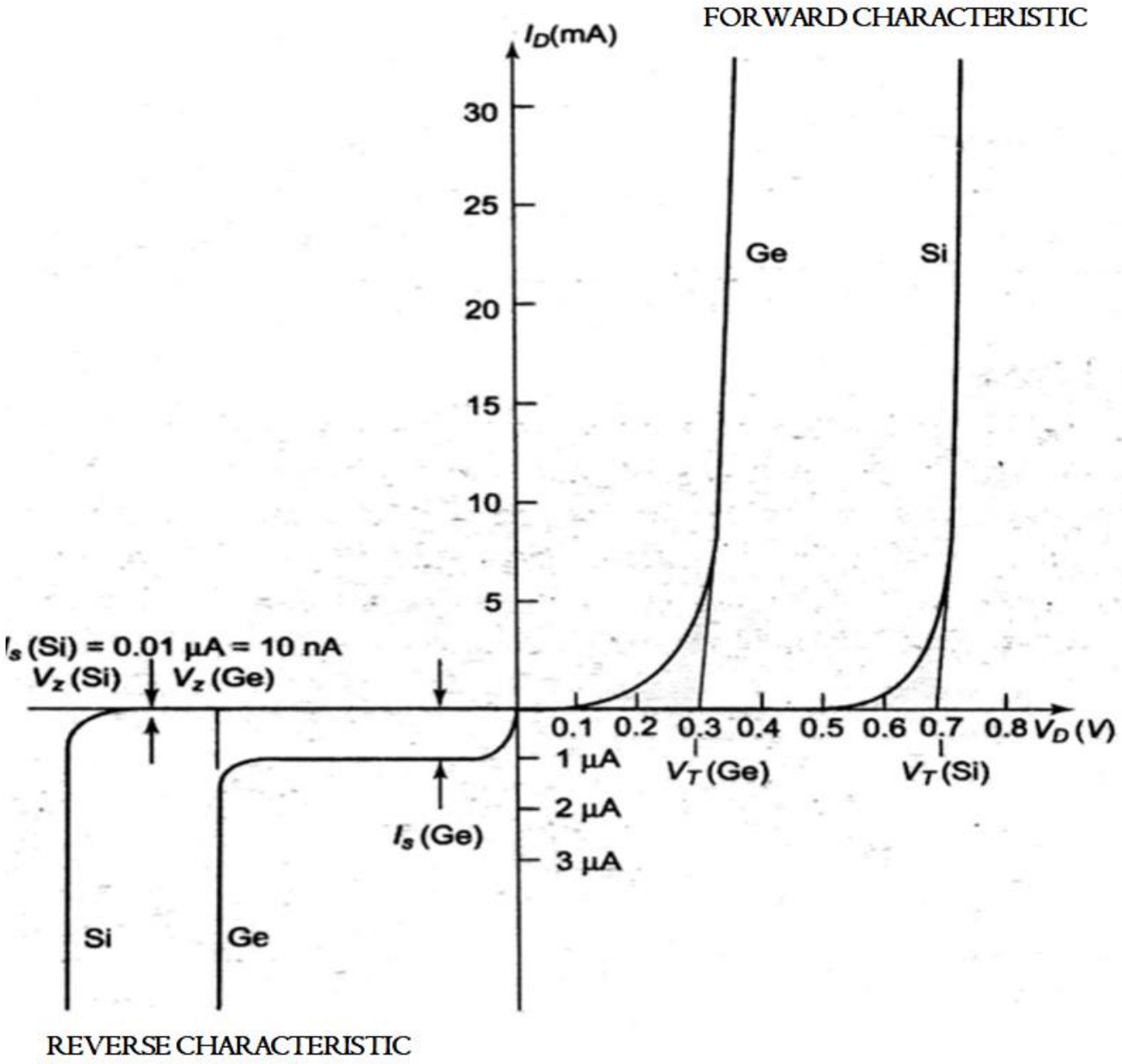




Reverse Biasing

- When the negative terminal of the battery is connected to the Anode (P-side) and positive terminal is connected to the Cathode (N-side), diode is said to be forward biased.
- As a result of reverse biasing, the majority of holes and electrons are pulled away from the junction, which increases the width of the depletion region.
- Therefore majority charge carrier current cannot flow, but minority carrier drift current flows which stays at saturation level which is very low.
- Reverse Saturation Current $\mathbf{I_s}$ will be in negligible order.

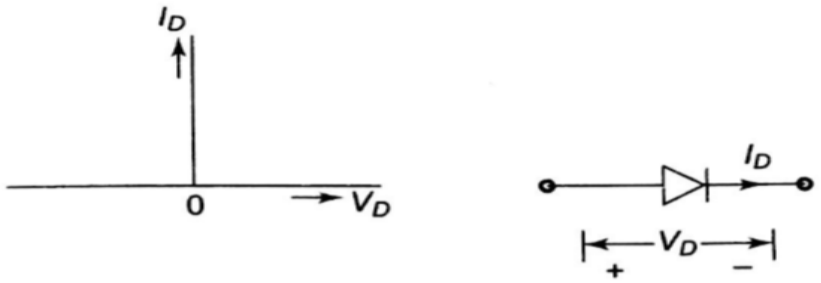



FORWARD CHARACTERISTIC
I_D(mA)
30
25
20
15
10
5
Ge
Si
I_s (Si) = 0.01 μA = 10 nA
V_z (Si)
V_z (Ge)
0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 V_D (V)
1 μA
2 μA
3 μA
V_T (Ge)
V_T (Si)
I_s (Ge)
Si
Ge
REVERSE CHARACTERISTIC

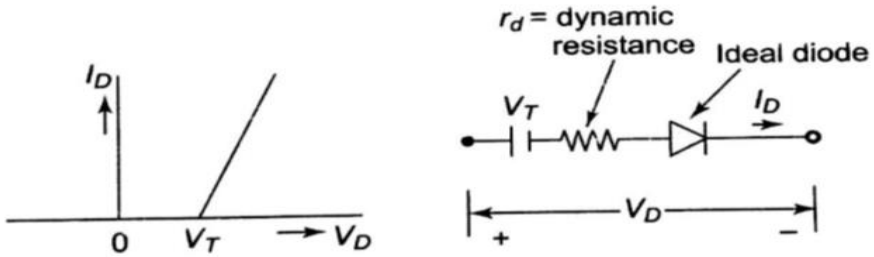
PN junction.mp4

Equivalent Circuits

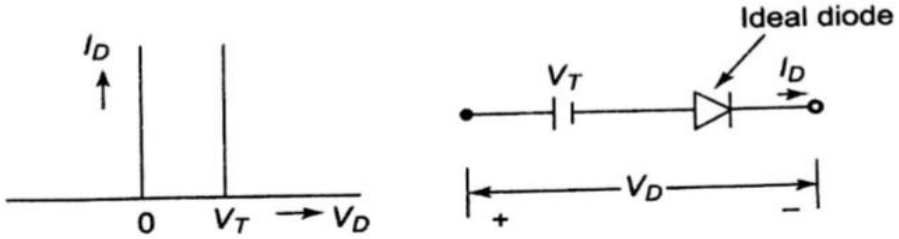
Ideal Diode: Diode which conducts when $\mathbf{V_D} > 0$ are called ideal diode.



Piecewise Linear Model: In this model, we consider the Diode Resistance ($\mathbf{r_d}$ _ Dynamic Resistance) with applied voltage above threshold voltage $\mathbf{V_T}$



Approximation Model: Assuming $r_d = 0$, the model characteristic and circuit are drawn as shown below.



Rectification

The process of converting AC to DC is called Rectification. An diode is an ideal and simple device to convert AC to DC.

There are two Types of Rectifiers:

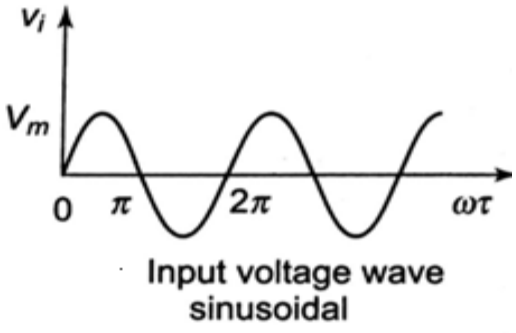
1. Half-Wave Rectifier
2. Full-Wave Rectifier

Here we measure the different parameters of Rectifier:

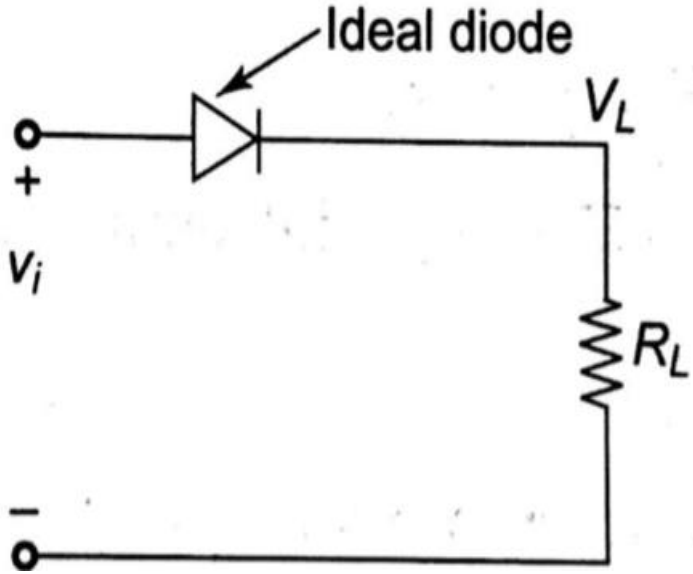
- DC Voltage
- Ripple Factor
- Power Conversion Efficiency
- PIV

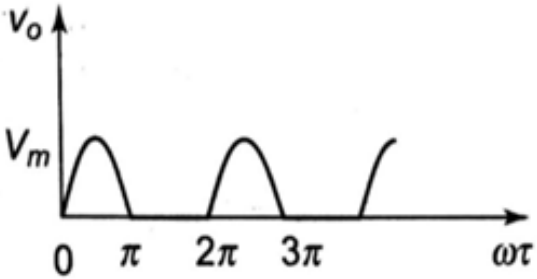
Half Wave Rectifier

- A Half-wave rectifier circuit consists of a diode and a resistor.
- For the given circuit, the diode conducts during the positive half cycles of the input and cuts off during the negative half cycles.
- Circuit is as shown below



Input voltage wave sinusoidal

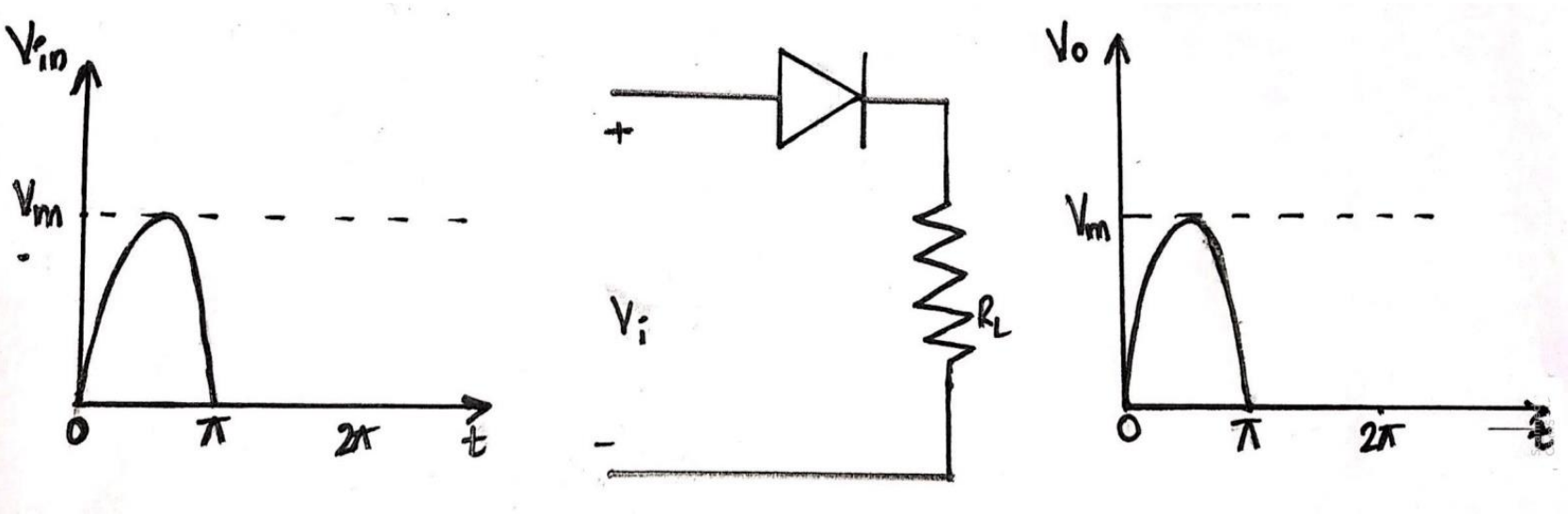




Output voltage wave

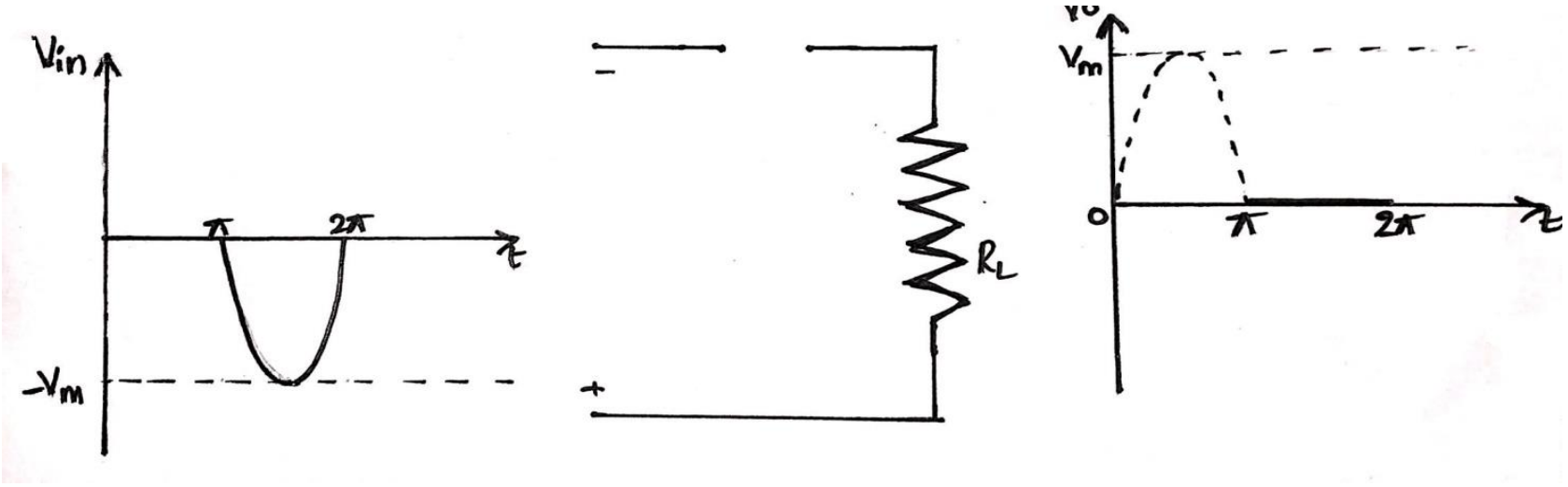
For the period: 0 – π

- We get positive half cycle of the sinusoidal input.
- Positive half cycle means positive voltage will be applied to the circuit.
- For positive voltage, the diode positive edge will be connected to the positive end of the supply and the resistor another end is connected to negative end of the supply.
- Hence the diode gets forward biased and it conducts producing the output for the same period.

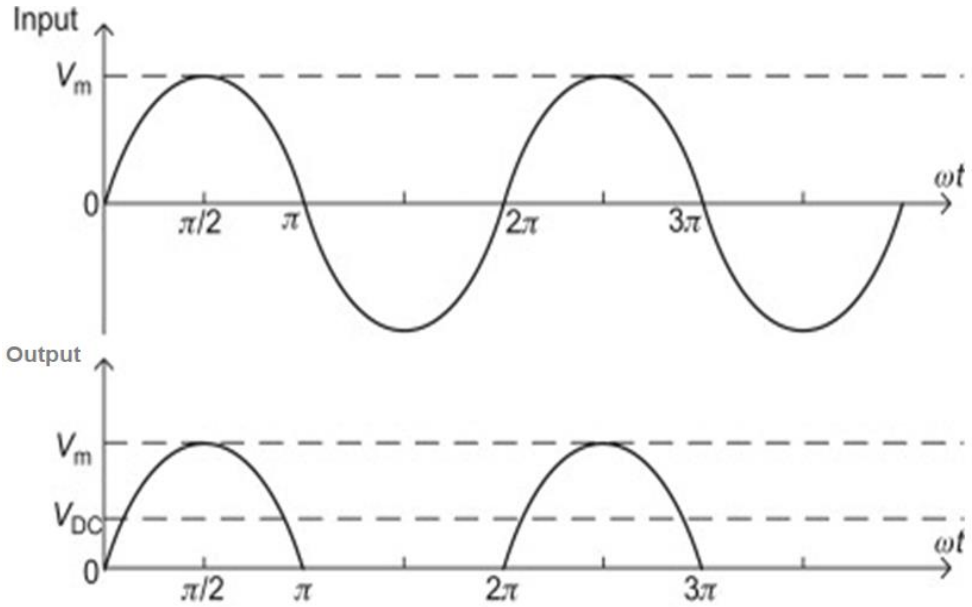


For the period : $\pi - 2\pi$

- We get the negative half cycle of the sinusoidal input.
- Negative half cycle means negative voltage will be applied to the circuit.
- For negative voltage, the diode positive edge will be connected to the negative end of the supply and the resistor another end is connected to positive end of the supply.
- The diode gets reverse biased and it does not conduct and the output is zero for the same period.



Input Output waveform of Half-wave rectifier is as shown below



Output Voltage:

$$V_{dc} = \frac{1}{2\pi}\left[V_m \int_0^{\pi} sin\omega t \, d\omega + 0 \right]$$

$$\mathbf{V_{dc}} = \frac{V_m}{\pi} = 0.318 * V_m$$

Output Current:

$$\mathbf{I_{dc}} = \frac{V_m}{\pi} * \frac{1}{R_L} \qquad = \frac{I_m}{\pi} \qquad = 0.318 * I_m$$

$$\mathbf{I_{dc}} = 0.318 * I_m$$

PIV for half wave rectifier is: **PIV = $\mathbf{V_m}$**

Ripple Factor of Half Wave Rectifier:

- Ripple is the variation of the output voltage about DC, which is high in Half-rectified wave.

- It has the frequency twice the frequency of the input voltage wave.

$$\textbf{Ripple Factor} \quad \gamma = \frac{rms\ value\ of\ the\ AC\ component\ of\ Load\ Voltage}{DC\ component\ of\ load\ voltage}$$

$$\gamma = \sqrt{\frac{V_{L\,rms}^2}{V_{L\,dc}^2} - 1}$$

$V_{L\ rms}$ = rms of half sine wave (0- π) over (0-2 π)

$$V_{L\,rms} = \sqrt{\frac{{V_m}^2}{\sqrt{2}^2} * \frac{1}{2}}$$

$$V_{L\ rms} = \frac{V_m}{2}$$

$$\gamma = \sqrt{\frac{(V_m/2)^2}{(V_m/\pi)^2} - 1}$$

$$= \left[\left(\frac{\pi}{2}\right)^2 - 1\right]^{1/2}$$

$$= 1.21$$

- We find that ripple factor of an half wave rectifier is quite higher, which is unacceptable.

- It is adjusted by the transformer output.

Power Conversion Efficiency of Half Wave Rectifier:

- It is defined as the ratio of DC power output and the AC power input.

$$\eta = \frac{DC\ Power\ Output}{AC\ Power\ Input}$$

DC Output = $I_{dc}^2 * R_L$

AC Input = $I_{rms}^2 * R_L$

$$I_{rms} = \sqrt{\frac{{I_m}^2}{\sqrt{2}^2} * \frac{1}{2}}$$

$$I_{rms} = \frac{I_m}{2}$$

$$\eta = \left[\frac{I_{dc}}{I_{rms}}\right]^2$$

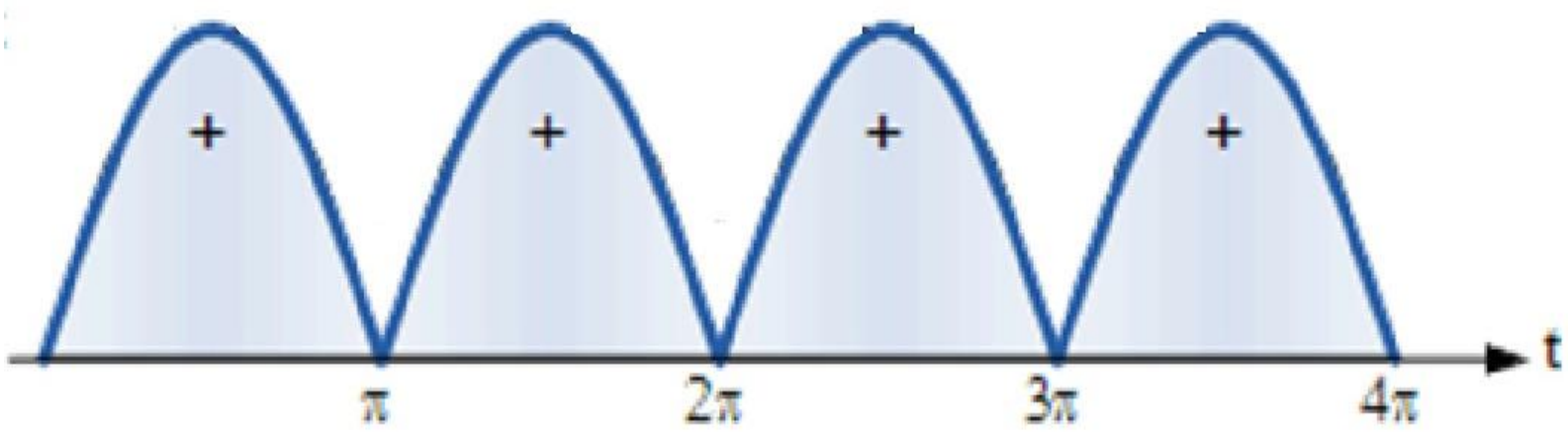
$$\eta = \left(\frac{I_m/\pi}{I_m/2}\right)^2$$

$$= (2/\pi)^2$$

$$= 0.405 \quad \text{or} \quad 40.5\%$$

Full wave Rectifier

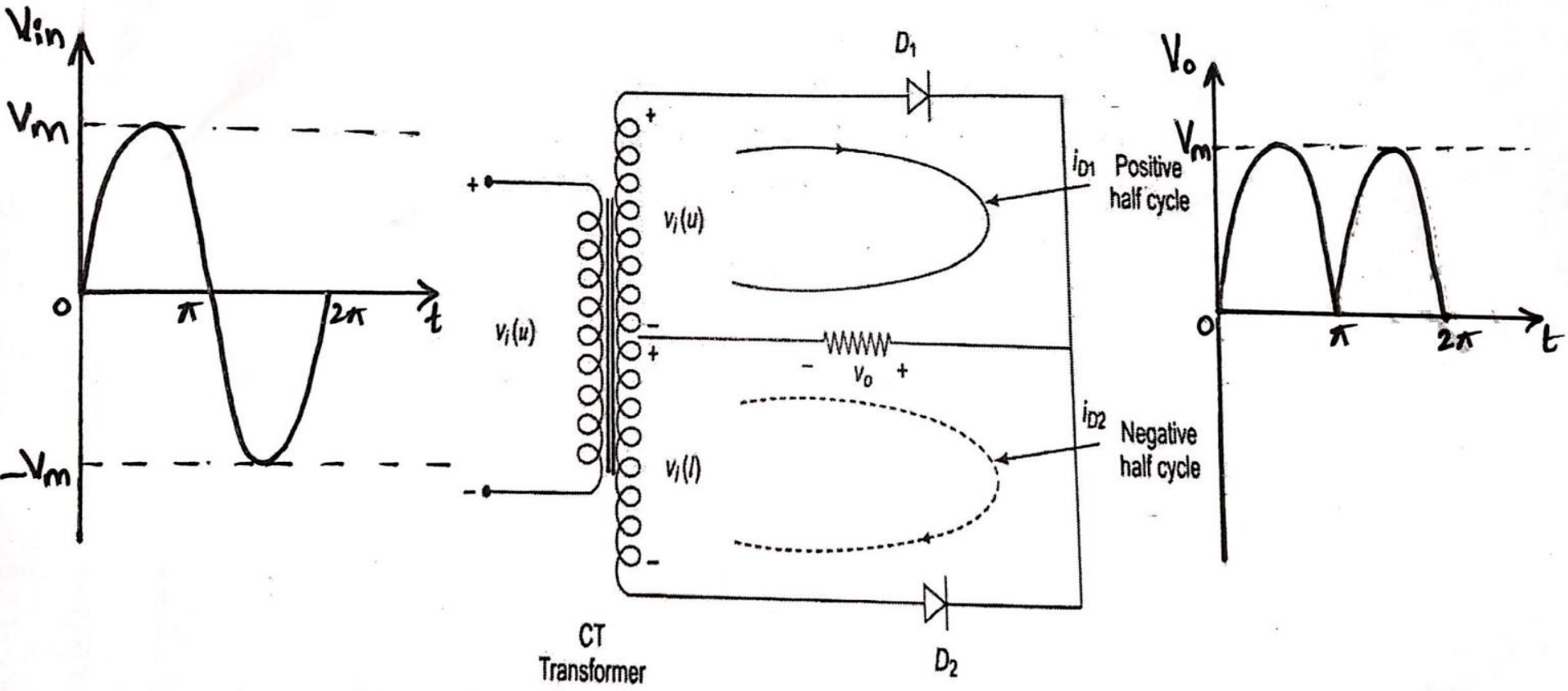
- In order to reduce the ripple factor and raise the output dc voltage level, we switch to full-wave rectification.
- Here we get the output for the complete one cycle of the input.
- At the output, phase of the second half of the wave is reversed.
- The full wave rectified output is as shown below:



Rectifier using Centre-Tapped (CT) Transformer:

The circuit consists of two diodes with a Centre Tapped transformer.

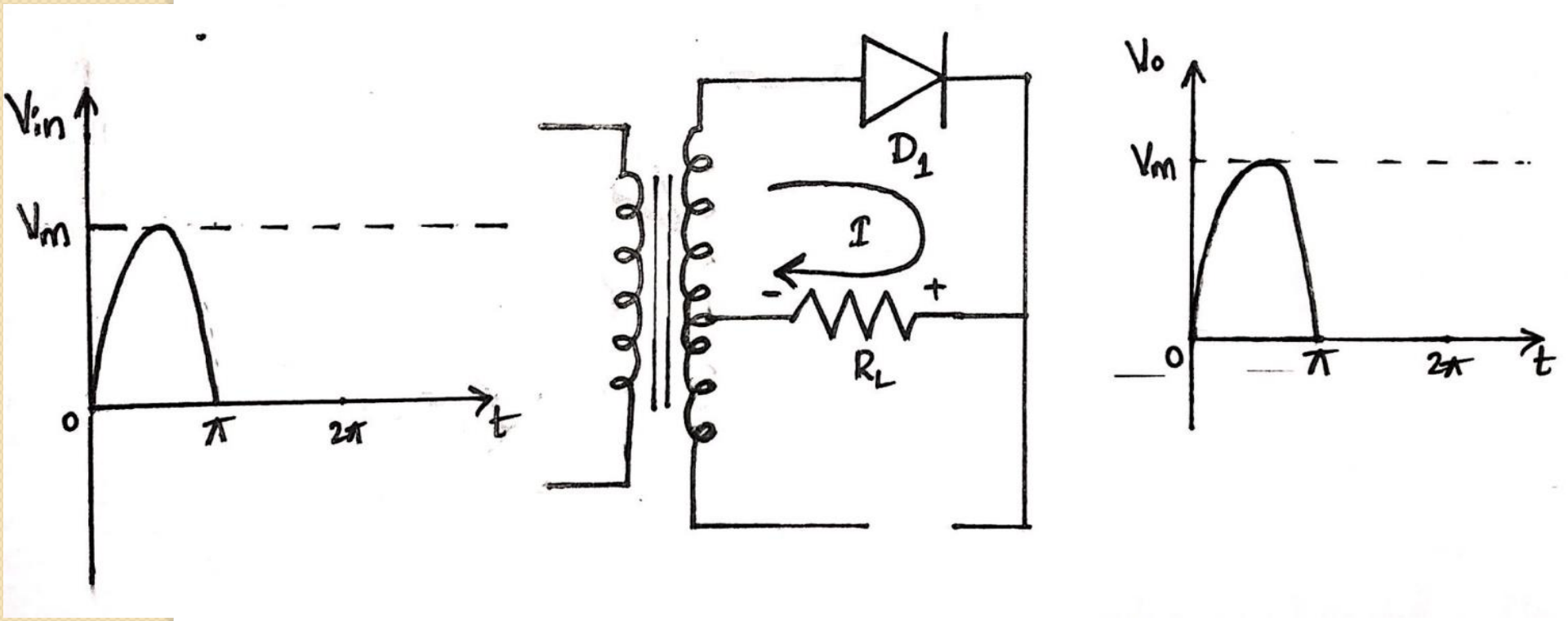
The network is as shown in the figure.



During the period of: 0 - π

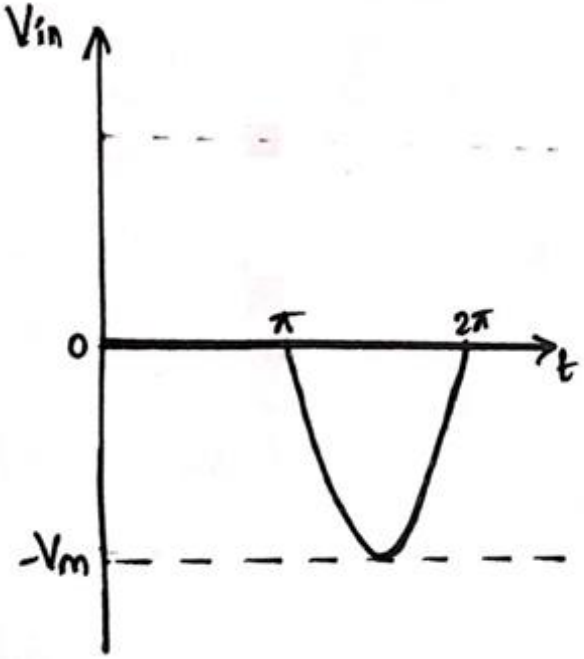
- We get positive half cycle of the sinusoidal input.

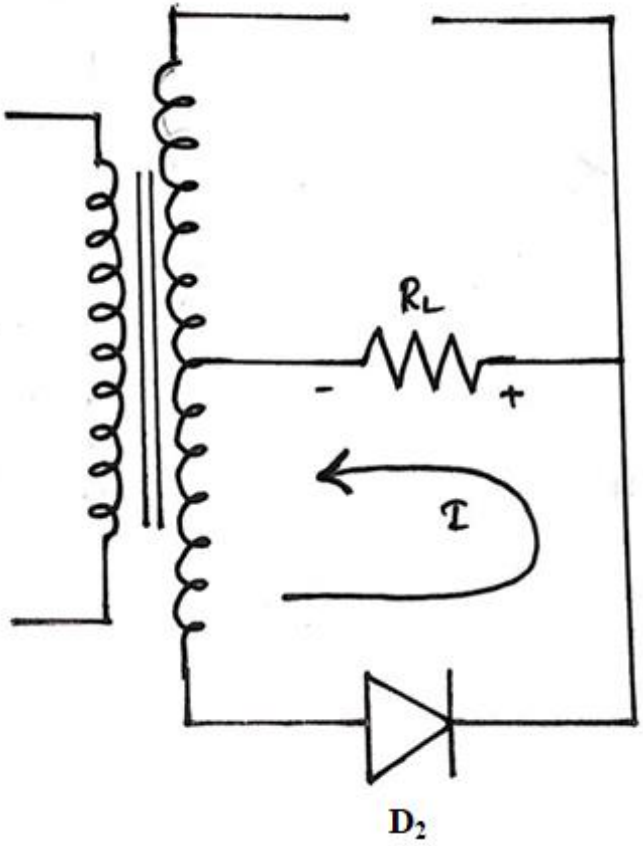
- The diodes $\mathbf{D_1}$ gets forward biased and it conducts through $\mathbf{R_L}$ producing the output for the same period. Diodes $\mathbf{D_2}$ gets reversed biased and it will be in the OFF state.

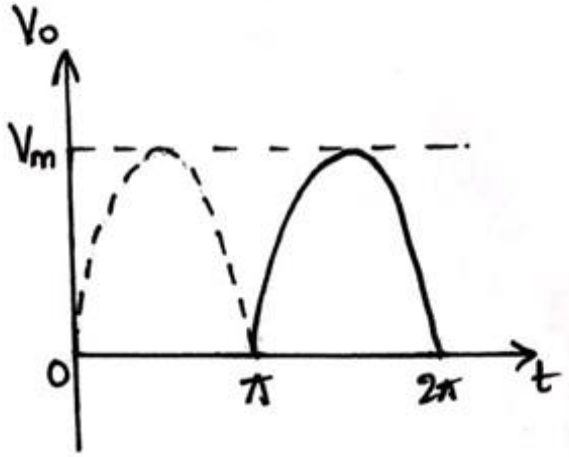


During the period of: π - 2π

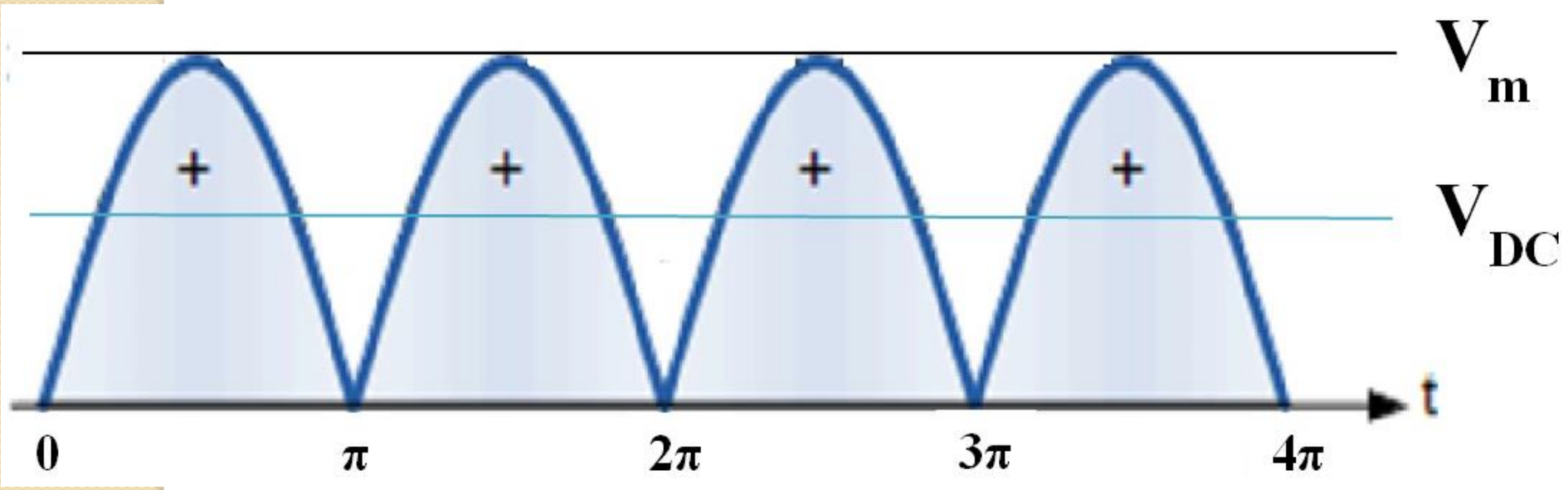
- We get negative half cycle of the sinusoidal input.
- The diodes $\mathbf{D_2}$ gets forward biased and it conducts through $\mathbf{R_L}$ producing the output for the same period. Diodes $\mathbf{D_1}$ gets reversed biased and it will be in the OFF state.







- Since the direction of flow of current through load resistance $\mathbf{R_L}$ remains same for both the half cycles, we get the positive output at $\mathbf{R_L}$.
- PIV voltage of Centre Tapped Transformer is: **PIV > $2V_m$**



Output Voltage:

$$V_{dc} = \frac{1}{2\pi}\left[\, 2V_m \int_0^{\pi} sin\omega t \, d\omega + 0 \,\right]$$

$$\mathbf{V_{dc}} = \frac{V_m}{\pi} = 0.318*2*V_m = \underline{0.636*V_m}$$

Output Current:

$$\mathbf{I_{dc}} = \frac{2V_m}{\pi} * \frac{1}{R_L} = \frac{2I_m}{\pi} = 0.318 * 2*I_m$$

$$\mathbf{I_{dc}} = 0.318 * *2*I_m = \underline{0.636*I_m}$$

PIV for half wave rectifier is: **PIV >2*V$_m$**

Ripple Factor of Full Wave Rectifier:

- Ripple is the variation of the output voltage about DC, which is high in Half-rectified wave.

- It has the frequency twice the frequency of the input voltage wave.

$$\textbf{Ripple Factor} \quad \gamma = \frac{rms\ value\ of\ the\ AC\ component\ of\ Load\ Voltage}{DC\ component\ of\ load\ voltage}$$

$$\gamma = \sqrt{\frac{V_{L\,rms}^2}{V_{L\,dc}^2} - 1}$$

$V_{L\ rms}$ = rms of full sine wave (0- 2π) over (0-2π)

$$V_{L\,rms} = \sqrt{\frac{V_m}{\sqrt{2}}^2}$$

$$V_{L\ rms} = \frac{V_m}{\sqrt{2}}$$

$$\gamma = \sqrt{\frac{(V_m/\sqrt{2})^2}{(2\,V_m/\pi)^2} - 1}$$

$$= \left[\frac{\pi^2}{8} - 1\right]^{1/2}$$

$$\gamma = 0.482$$

- We find that ripple factor of an full wave rectifier is less than the half wave rectifier.

Power Conversion Efficiency of Full Wave Rectifier:

- It is defined as the ratio of DC power output and the AC power input.

$$\eta = \frac{DC\ Power\ Output}{AC\ Power\ Input}$$

DC Output = $I_{dc}^2 * R_L$

AC Input = $I_{rms}^2 * R_L$

$$I_{rms} = \sqrt{\frac{I_m}{\sqrt{2}}^2}$$

$$= \frac{I_m}{\sqrt{2}}$$

$$I_{rms} = \frac{I_m}{\sqrt{2}}$$

$$\eta = \left[\frac{I_{dc}}{I_{rms}}\right]^2$$

$$\eta = \left(\frac{2I_m/\pi}{I_m/\sqrt{2}}\right)^2$$

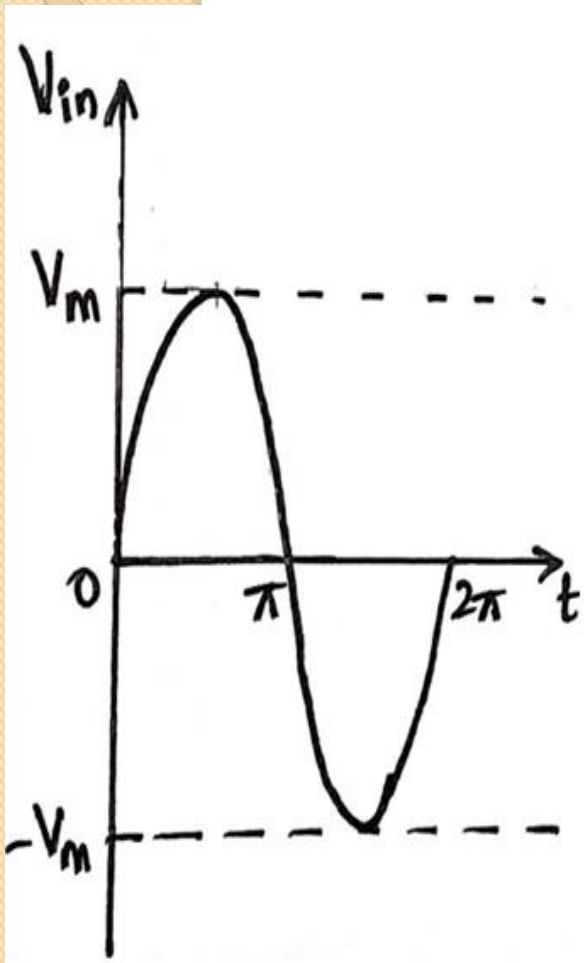
$$= (2\sqrt{2}/\pi)^2$$

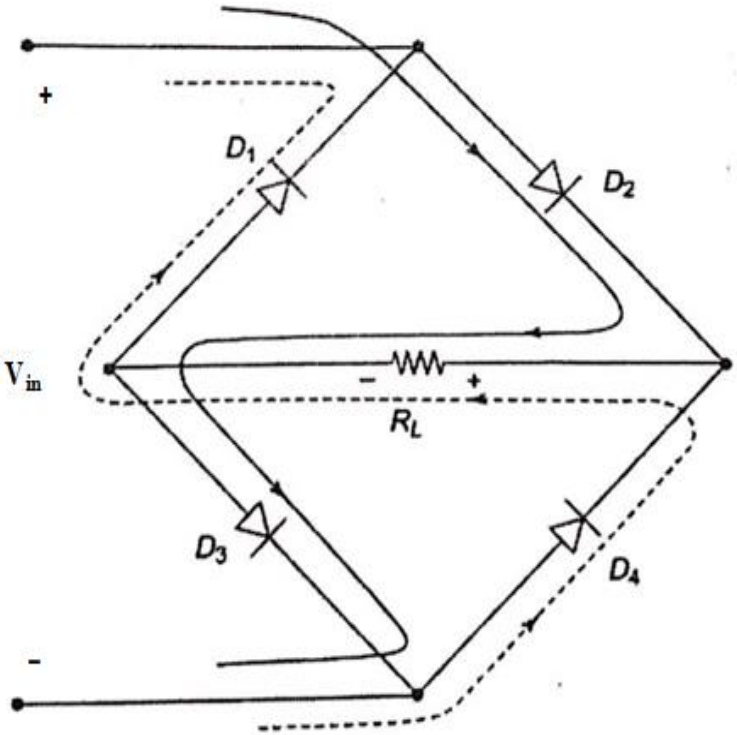
$$= 0.81 \quad \text{or} \quad 81\%$$

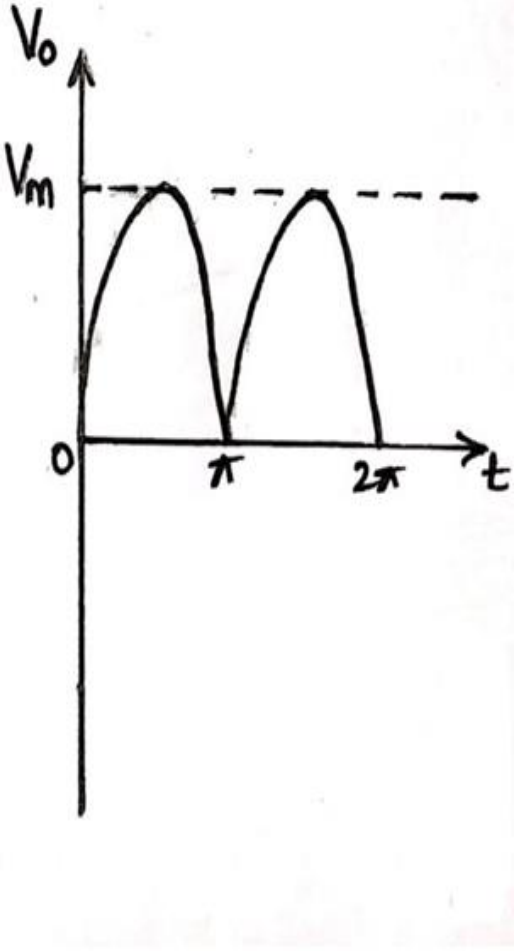
Bridge Rectifier:

The circuit consists of 4 diodes which forms the bridge structure.

It is the most common full-wave rectifier circuit used.

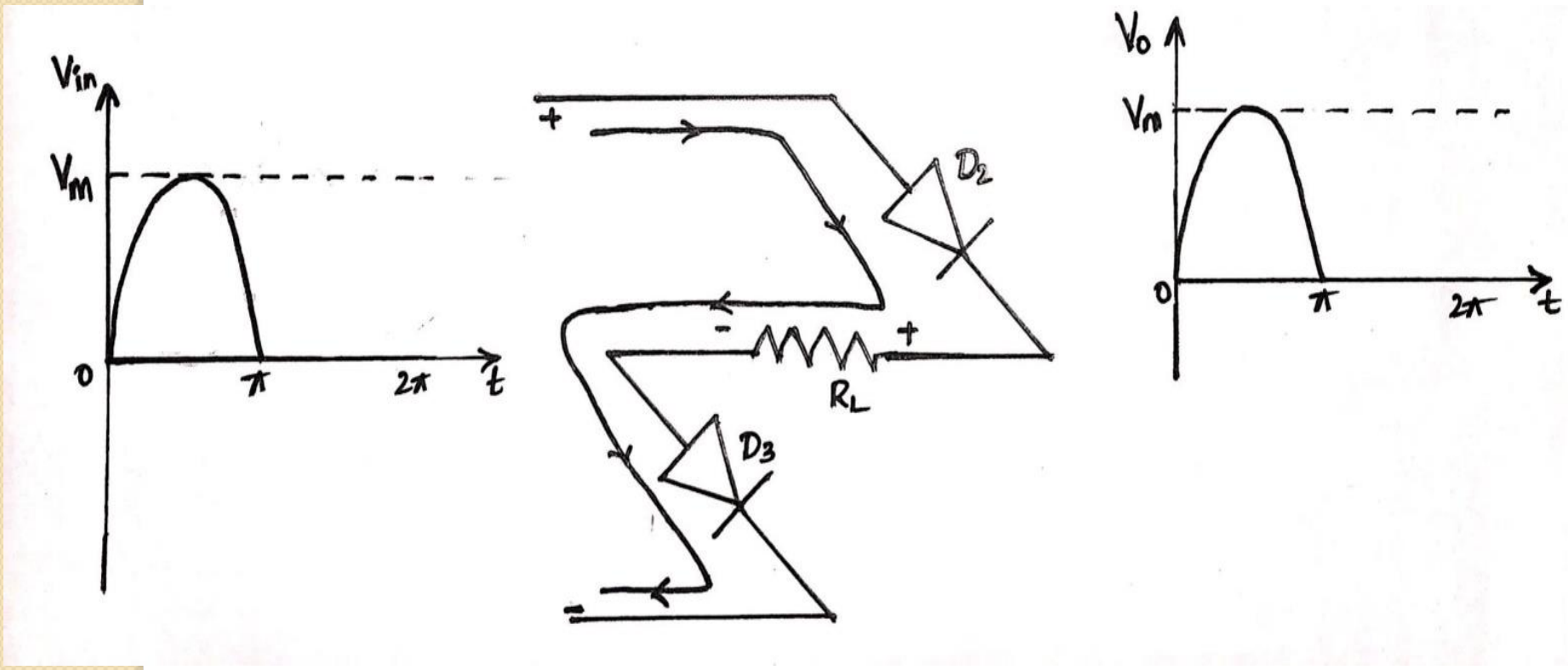






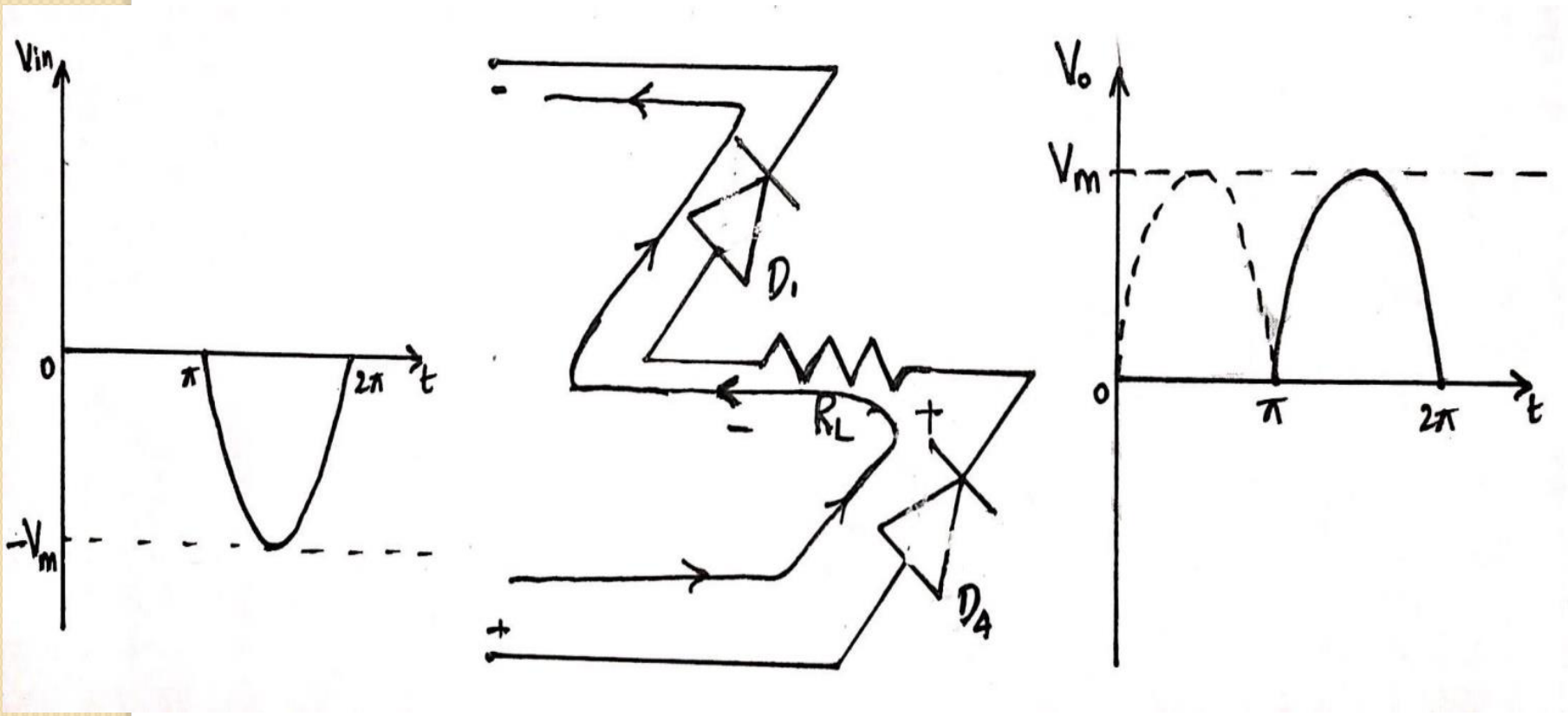
During the period of: 0- π

- We get positive half cycle of the sinusoidal input.
- The diodes $\mathbf{D_2}$ and $\mathbf{D_3}$ gets forward biased and it conducts through $\mathbf{R_L}$ producing the output for the same period. Diodes $\mathbf{D_1}$ and $\mathbf{D_4}$ gets reversed biased and it will be in the OFF state.

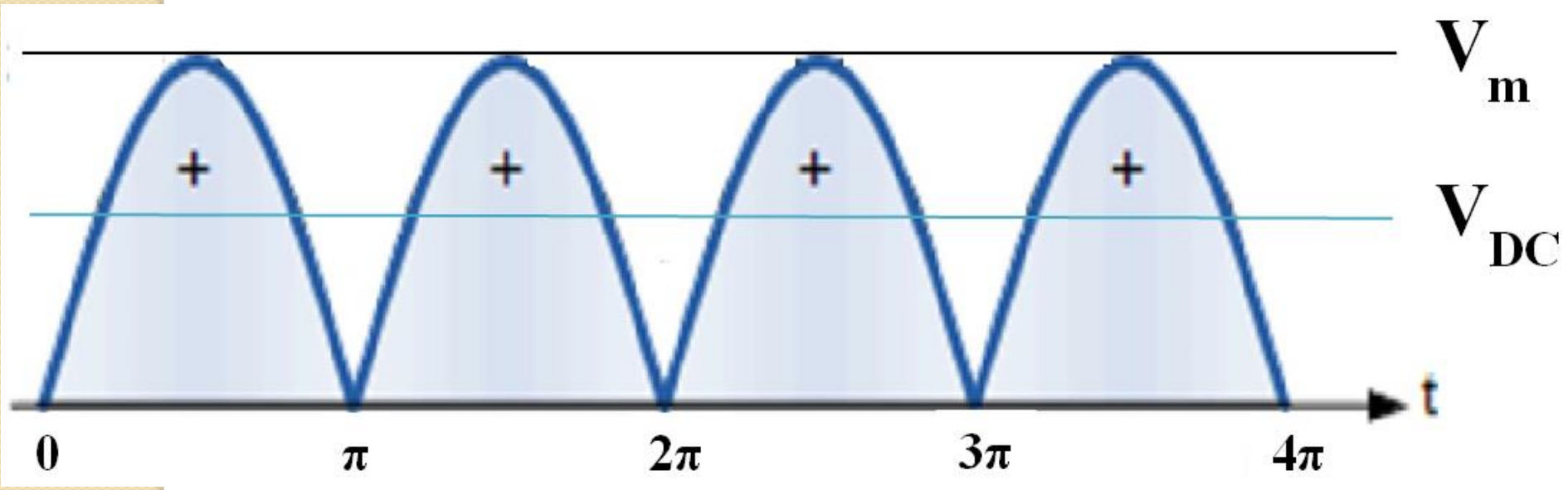


During the period of: $\pi - 2\pi$

- We get positive half cycle of the sinusoidal input.
- The diodes $\mathbf{D_1}$ and $\mathbf{D_4}$ gets forward biased and it conducts through $\mathbf{R_L}$ producing the output for the same period. Diodes $\mathbf{D_2}$ and $\mathbf{D_3}$ gets reversed biased and it will be in the OFF state.

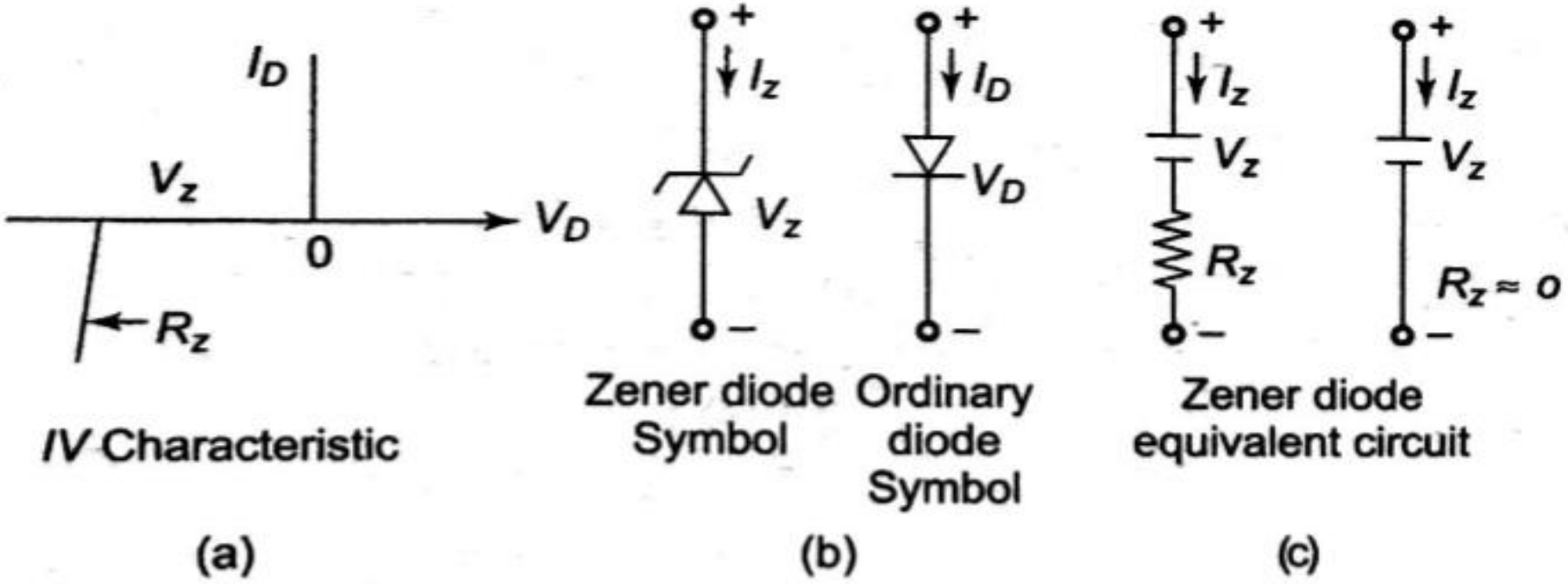


- Since the direction of flow of current through load resistance $\mathbf{R_L}$ remains same for both the half cycles, we get the positive output at $\mathbf{R_L}$.
- PIV voltage of Centre Tapped Transformer is: **PIV > $2V_m$**



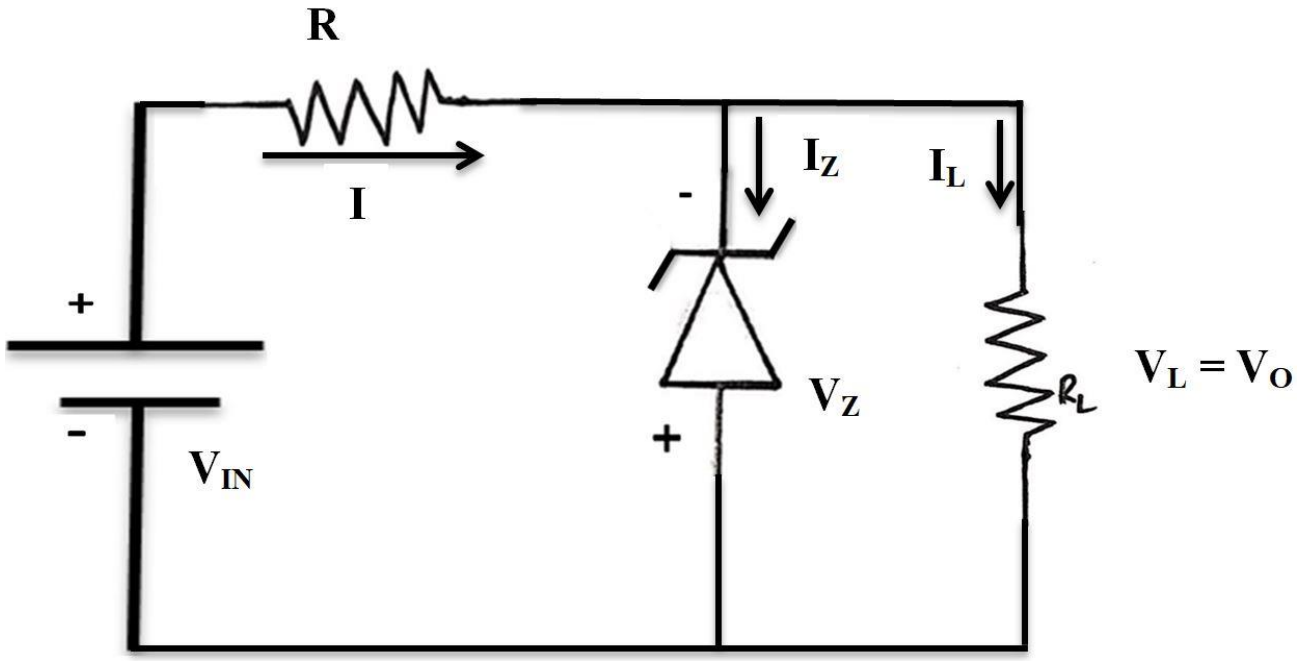
Zener Diode:

- Zener diode has zero breakdown in reverse bias as shown in VI characteristics of figure **a**.
- The symbol of the Zener diode is drawn in figure **b.** Its equivalent circuit is drawn in figure **c.**
- It is connected in circuit such that it is reverse biased. It conducts only if reverse bias exceeds $\mathbf{V_z}$.

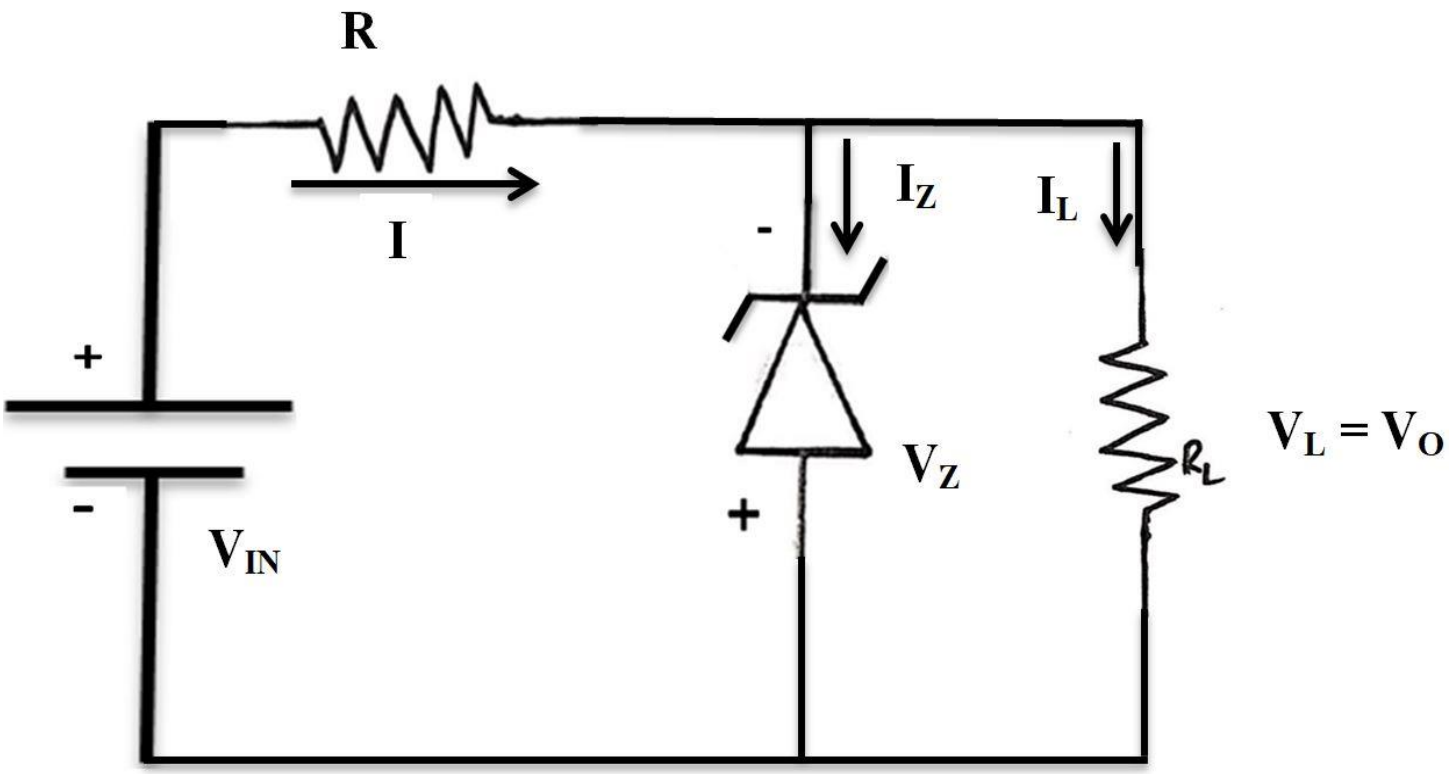


Zener Diode as a Voltage Regulator:

- Voltage regulators are the devices used to maintain constant voltage across load , despite of fluctuations in the input voltage and load current.
- The Zener diode in its reverse region, it is widely used as voltage regulator as it continues to operate till the magnitude of current becomes less than $\mathbf{I_{Z(min)}}$.
- The typical Zener voltage regulator is shown in figure below.



- The Zener diode of breakdown voltage V_Z is connected to the input supply in reverse direction.
- For all the values of current within the breakdown region, the voltage across the diode will remain fixed at V_Z, giving a constant supply across its load.
- The resistance R_S controls the current flowing in the circuit.



Line Regulation:

- In this case, **load resistance is kept constant** and **input voltage (V_{in}) is varied.**
- The regulated output voltage is achieved for input voltage above certain minimum level.
- It can be seen that the output is $\mathbf{V_O = V_Z}$ is constant.
- $\mathbf{I_L}$ is given by; $\mathbf{I_L = \frac{V_O}{R_L} = \frac{V_Z}{R_L} = constant}$
- Total $\mathbf{I = I_Z + I_L}$

- Now if $\mathbf{V_{in}}$ **increases**, then the total current **I increase**.
- But $\mathbf{I_L}$ is constant as $\mathbf{V_Z}$ is constant.
- Hence the current $\mathbf{I_Z}$ **increases** to keep $\mathbf{I_L}$ constant. (I_L is constant, I increases, I_Z becomes Maximum (I_{Zmax})).

- For $\mathbf{V_{in}}$**= Maximum**;

$$\mathbf{I = I_{Zmax} + I_L} \qquad \mathbf{I_{Zmax} = I - I_L}$$

- Now if $\mathbf{V_{in}}$ **decreases**, then the total current **I decrease**.
- Since $\mathbf{V_Z}$ is constant, hence the current $\mathbf{I_Z}$ **decreases** to keep $\mathbf{I_L}$ **constant**. (I_L is constant, I decreases, I_Z becomes Minimum (I_{Zmin}))

- For $\mathbf{V_{in}}$**= Minimum**;

$$\mathbf{I = I_{Zmin} + I_L} \qquad \mathbf{I_{Zmin} = I - I_L}$$

- As long the $\mathbf{I_Z}$ value is between $\mathbf{I_{Zmin}}$ and $\mathbf{I_{Zmax}}$, output voltage $\mathbf{V_O}$ will be constant.

Load Regulation:

- In this case **the input voltage is fixed** while the **load resistance is varied**.

- The constant output voltage is obtained as long as the load resistance is maintained above a minimum value.

- Since $\mathbf{V_O = V_Z}$ is constant, then for constant **R**, **I** is given by;

$$\mathbf{I} = \frac{V_{in} - V_z}{R} = \mathbf{I_Z + I_L}$$

- Now if **R_L decreases**, then **I_L increases**.
- To keep **I constant, I_Z decreases**. (I is constant, I_L increases, I_Z becomes Minimum (I_{Zmin})).
- For **R_L= Minimum;**

  I_L is Maximum **$I = I_Z + I_{Lmax}$** **$I_{Zmin} = I – I_{lmax}$**

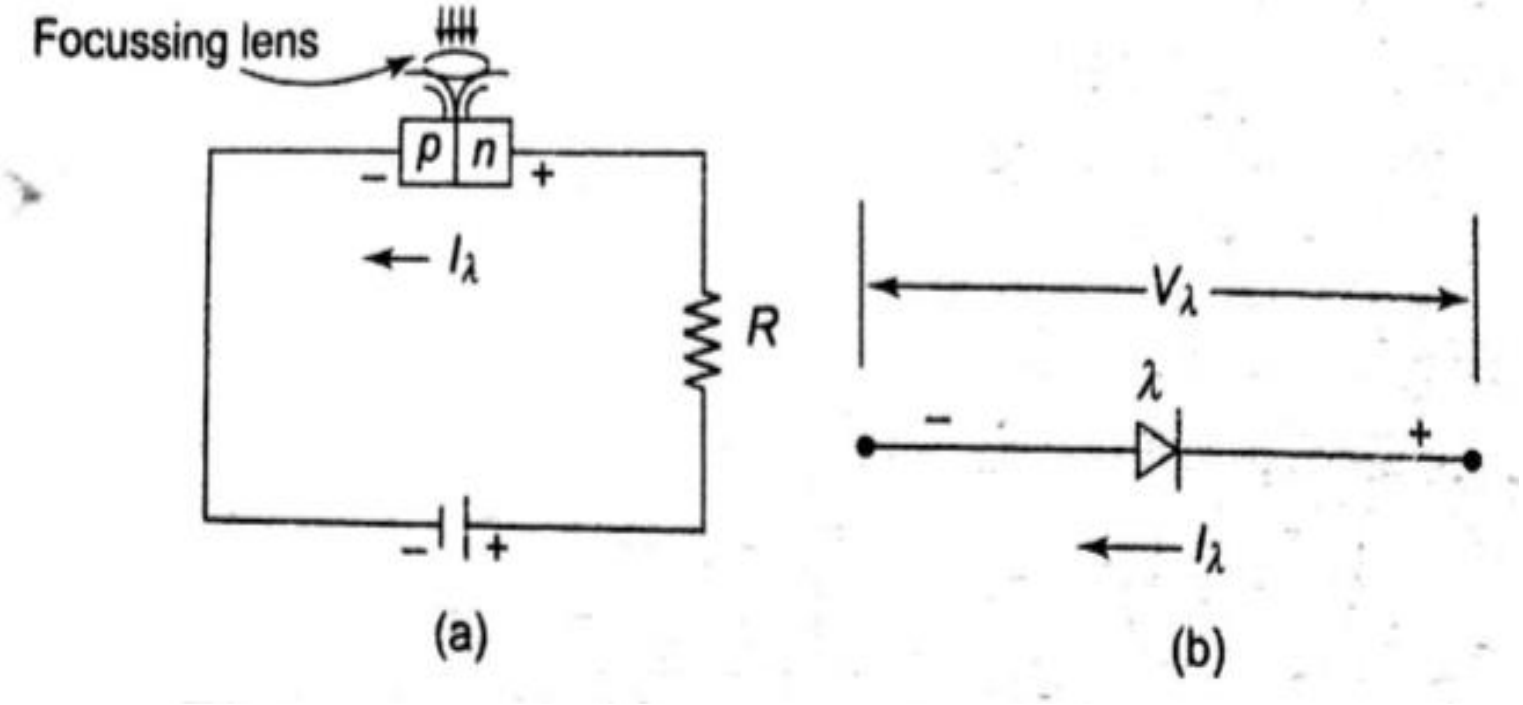
- Now if **R_L increases**, then **I_L decreases**.
- To keep **I constant, I_Z increases**. (I is constant, I_L decreases, I_Z becomes Maximum (I_{Zmax})).
- For **R_L= Maximum;**

  I_L is Minimum **$I = I_Z + I_{Lmin}$** **$I_{Zmax} = I - I_{Lmin}$**

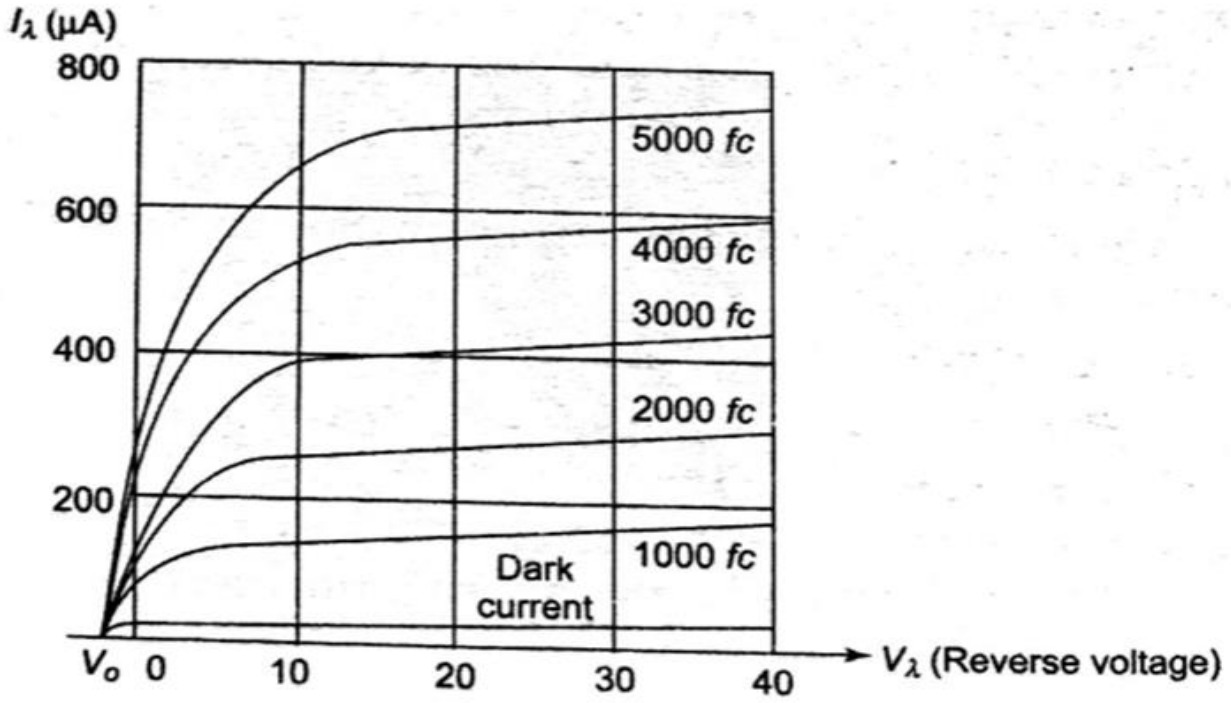
- As long the I_Z value is between I_{Zmin} and I_{Zmax}, output voltage V_O will be constant.

Photo Diode:

- Photodiode is a semiconductor PN-junction device whose region of operation is limited to the reverse bias region.
- The biasing arrangement, construction and symbol for the device is as follows:



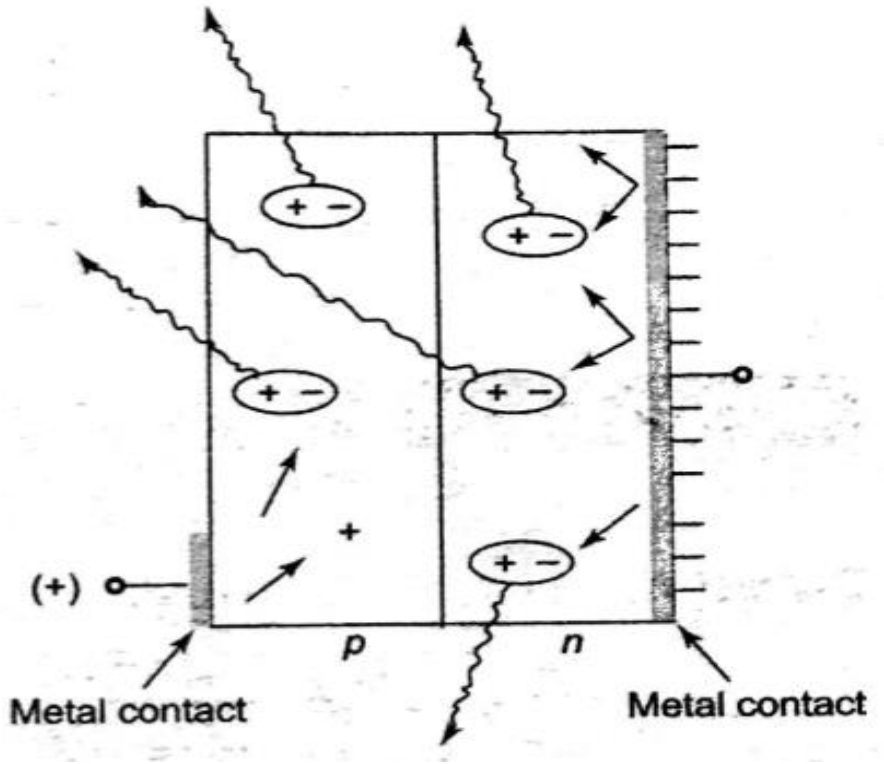
- Reverse saturation current is normally limited to a few micro amperes.
- The application of light to the junction will result in a transfer of energy from the incident travelling light waves to the atomic structure, resulting in an increased number of minority carriers and an increased level of reverse current.
- "Dark current is the current that will exist with no applied illumination".
- That is shown in below figure for different intensity levels,



***Light Emitting Diode* [LED]:**

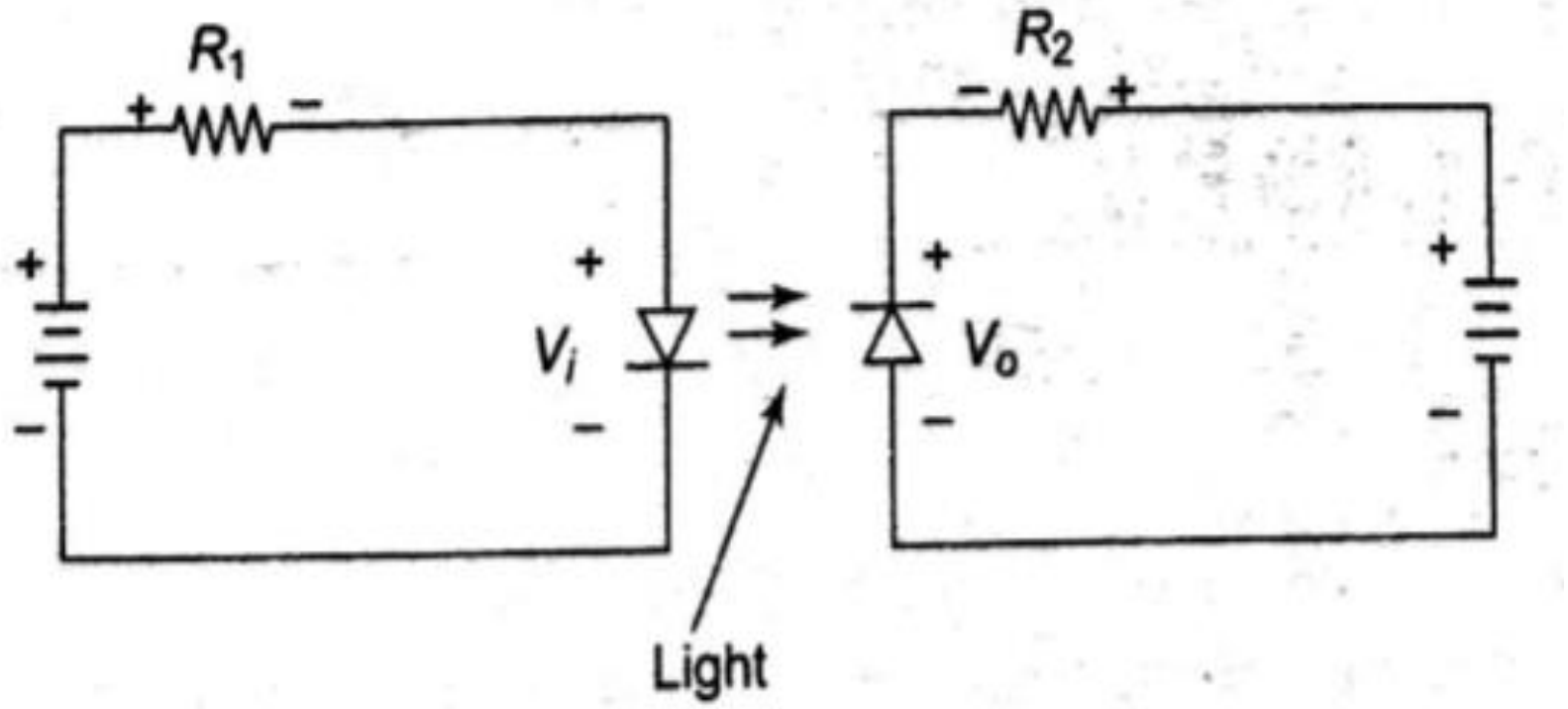
- In a forward bias PN-junction, diode recombination of electrons and holes takes places at the junction and within the body of the crystal, particularly at the location of a crystal defect.
- Upon capture of a free electron by a hole, the electron goes into a new state and its kinetic energy is given off as heat and as light photons.
- In a silicon diode, most of this energy is given off as heat but in other materials such as Gallium Arsenide (GaAS) or Gallium Phosphide (GaP), sufficient numbers of photons (light) are generated so as to create a visible source.
- This process of light emission in PN-junction of such materials is illustrated in the figure below and is known as ***Electroluminescence***.
- The metal contact of P-material is made much small to permit the emergence of maximum number of photons so that in an LED, the light lumens generated per watt of electric power is quite high.

- Intensity of light increases almost linearly with forward current, depending on the material used.
- The voltage levels of LEDs are 1.7V to 3.3V which is compatible with the solid state circuits.
- LEDs have short response time and light contrast is good.
- LEDs emit light red, green, orange or blue.

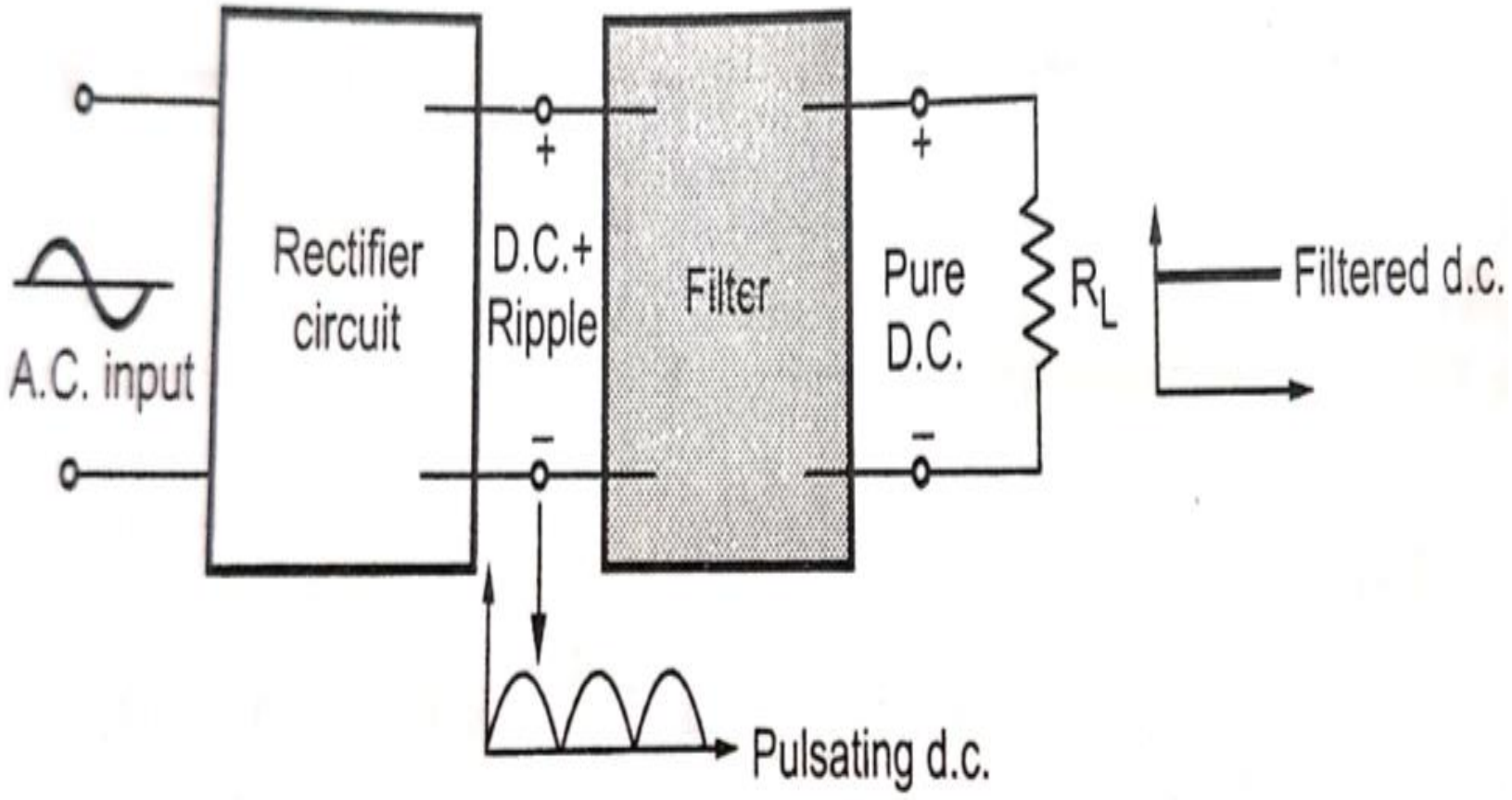


Photocoupler:

- It is a package of an LED and photodiode whereas circuits are electrically isolated as shown in figure below.
- The LED is forward biased and the photodiode is reverse biased. The output is available across R_2.

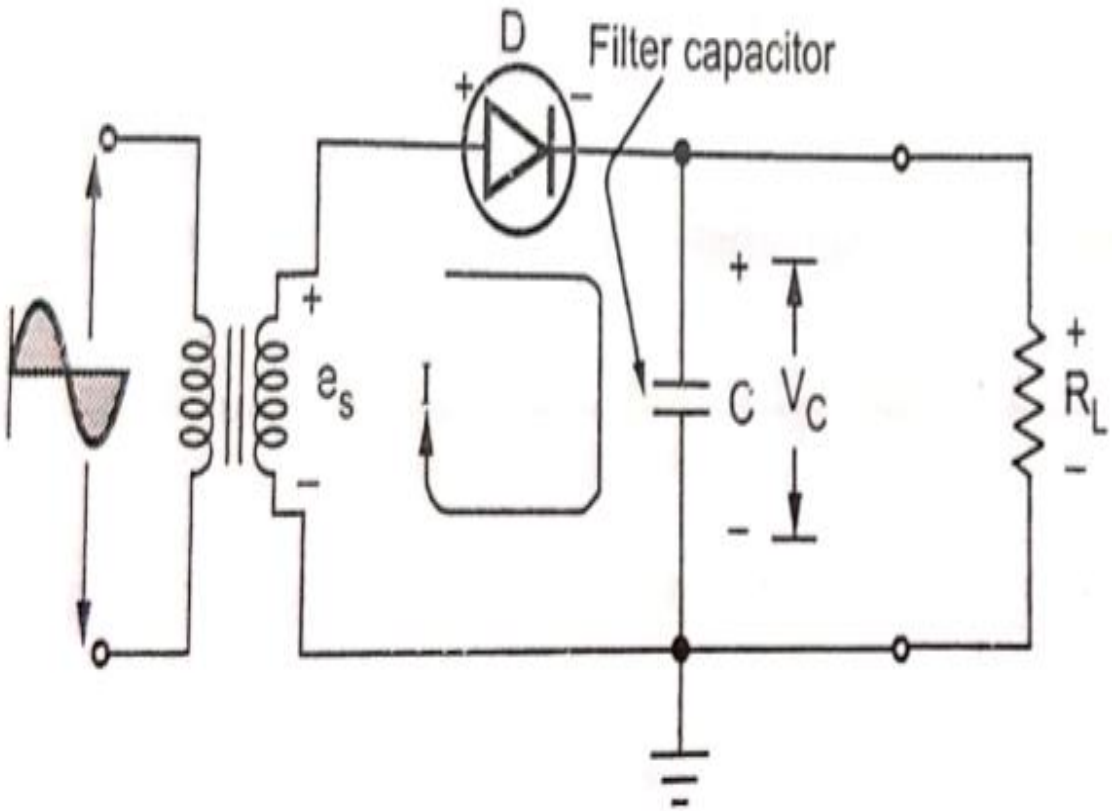


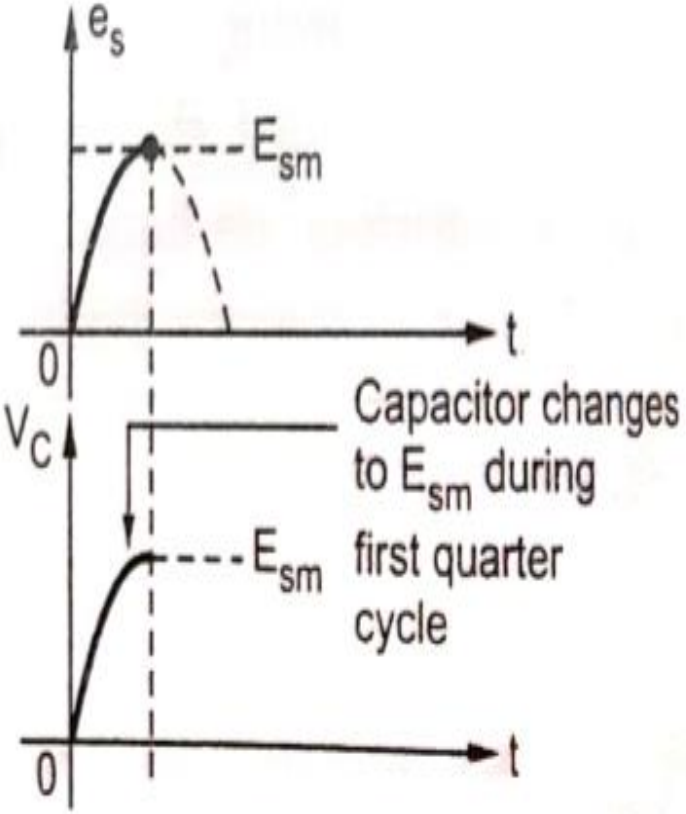
Capacitor Filter Circuit:



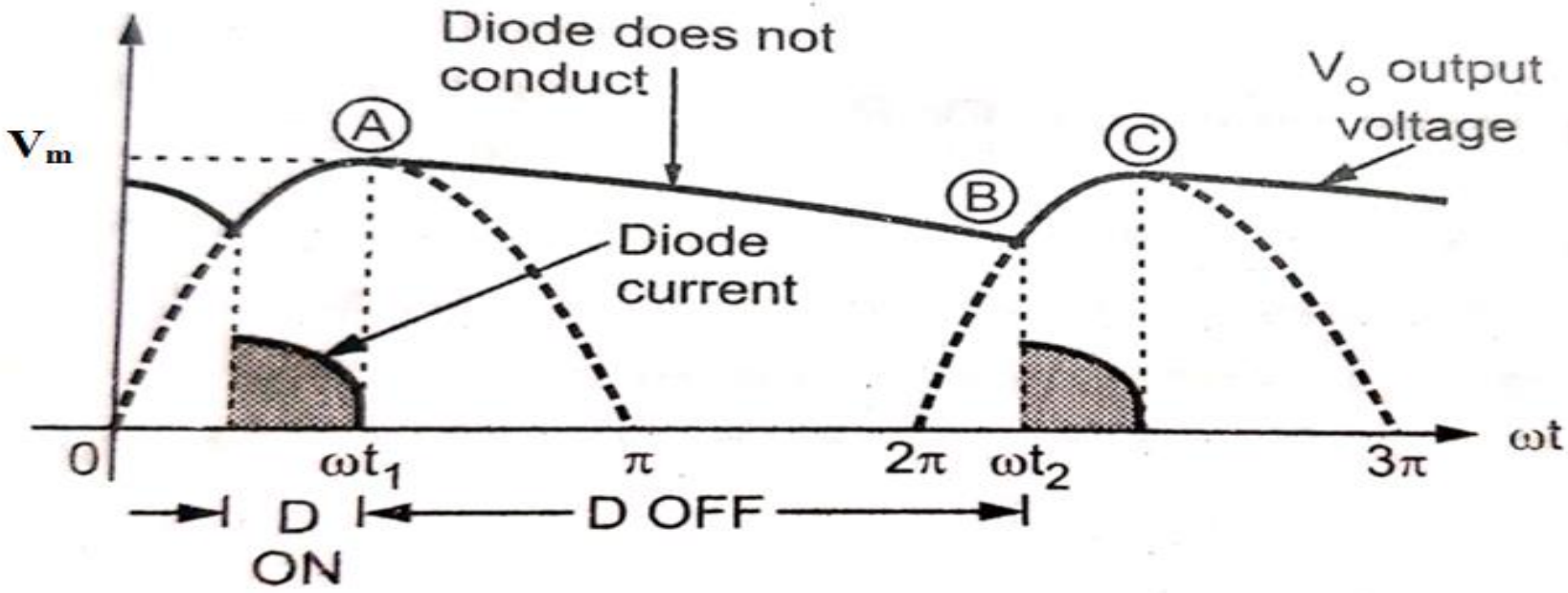
- The output of a half-wave and full-wave rectifier circuit is not pure DC which contains ripples.
- To minimize the ripple in the output, filters circuit are used.
- Filter circuits are connected between the rectifier and the load as shown in the figure.
- An AC input is applied to the rectifier circuit which produces the DC voltage output with ripple voltage.
- This will be fed as an input to the filter circuit which produces the pure DC by minimizing the ripple voltage.
- Usually capacitor is used as an filter element.

Half Wave Rectifier with capacitor filter:





- Figure above shows an half wave rectifier with capacitor input filter.
- Filter uses a single capacitor connected in parallel with the load.
- During the positive half cycle of the input, the diode is forward biased and this charges the capacitor C to the peak value of the input V_m.
- When input starts decreasing the peak value V_m, the capacitor remains charged at V_m and the diode gets reverse biased due to capacitor voltage.
- Hence during the complete negative half cycle and for some part of positive half cycle capacitor discharges through R_L as sown in the figure below.



- The voltage is same as the output voltage as it is in parallel with R_L.
- From the above figure it can be seen that diode conducts only from point **B** to **C** where capacitor gets charged to V_m. Thus diode gets forward biased.
- From point **A** to **B,** the diode remains non-conducting and conducts only for the period from **B** to **C**.
- Diode Current will be present for the period when diode is conducting.

Ripple Factor of Half wave Rectifier with filter:

- RMS value of output of capacitor filter circuit is given by:

$$\mathbf{V_{RMS}} = \frac{V_R}{2\sqrt{3}}$$

Where: V_R – Peak to Peak Ripple voltage

- During the time interval T_2 the capacitor C discharges through R_L. the charge discharged is given by:

$$\mathbf{Q = CV_R}$$

$$\mathbf{i} = \frac{dQ}{dt}$$

$$\mathbf{Q} = \int_0^{T_2} i\, dt$$

$$\mathbf{Q = I_{DC} * T_2}$$

Average output or DC voltage is given by:

$$\mathbf{I_{DC} * T_2 = C V_R}$$

$$V_R = \frac{I_{DC} T_2}{C}$$

$T_2 = T$ since $T_1 + T_2 = T$ and $T_2 \gg T_1$ and $T = 1 / f$

$$V_R = \frac{I_{DC}\, T}{C} = \frac{I_{DC}}{fC}$$

$$I_{DC} = \frac{V_{DC}}{R_L}$$

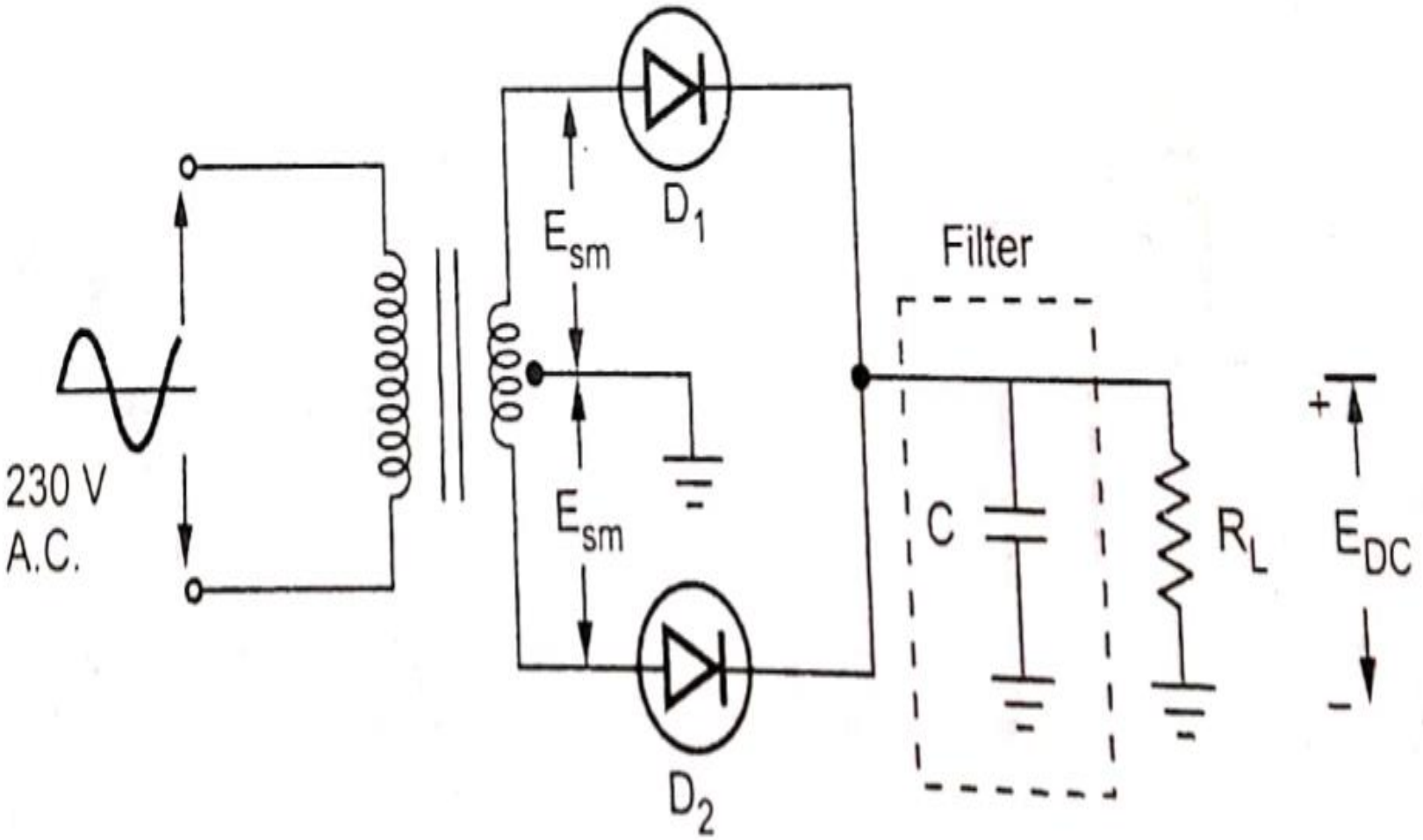
$$V_R = \frac{V_{DC}}{fCR_L}$$ peak to peak Ripple Voltage

$$\text{Ripple Factor} = \frac{V_{RMS}}{V_{DC}} = \frac{\frac{V_R}{2\sqrt{3}}}{V_{DC}}$$

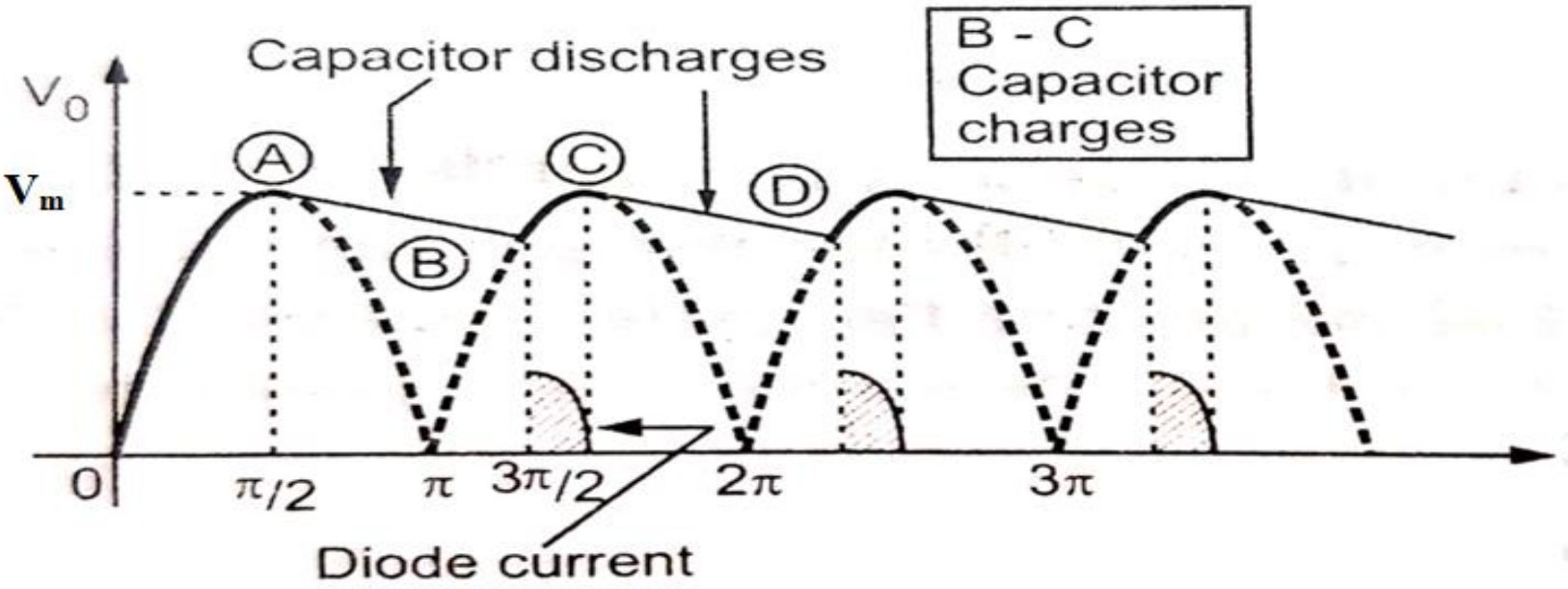
$$= \frac{V_{DC}}{V_{DC}\, 2\sqrt{3}\, fCR_L}$$

$$\textbf{Ripple Factor} = \frac{1}{2\sqrt{3}\, fCR_L}$$

Full Wave Rectifier with capacitor filter:



- Figure above shows an half wave rectifier with capacitor input filter.
- Filter uses a single capacitor connected in parallel with the load.
- During the positive half cycle of the input, the diode **D_1** is forward biased and this charges the capacitor C to the peak value of the input V_m.
- Once the diode is charged to V_m, the diode **D_1** becomes reverse bias and stops conducting and capacitor discharges until **B**.
- Once the capacitor gets the threshold value, capacitor gets charged to peak value V_m i.e. from **B** to **C.**



- During time T_1, capacitor gets charged and this process is quick.
- During time T_2, capacitor gets discharged through $\mathbf{R_L}$ slowly and hence $T_2 \gg T_1$
- Diode Current will be present for the period when diode is conducting.

Ripple Factor of Full wave Rectifier with filter:

- RMS value of output of capacitor filter circuit is given by:

$$\mathbf{V_{RMS}} = \frac{V_R}{2\sqrt{3}}$$

Where: V_R – Peak to Peak Ripple voltage

- During the time interval T_2 the capacitor C discharges through R_L. the charge discharged is given by:

$$\mathbf{Q = CV_R}$$

$$\mathbf{i} = \frac{dQ}{dt}$$

$$\mathbf{Q} = \int_0^{T_2} i\, dt$$

$$\mathbf{Q = I_{DC} * T_2}$$

Average output or DC voltage is given by:

$$\mathbf{I_{DC} * T_2 = C V_R}$$

$$V_R = \frac{I_{DC} T_2}{C}$$

$T_2 = T/2$ since $T_1 + T_2 = \frac{T}{2}$ and $T_2 \gg T_1$ and $T = 1/f$

$$V_R = \frac{I_{DC}\, T}{2C} = \frac{I_{DC}}{2fC}$$

$$I_{DC} = \frac{V_{DC}}{R_L}$$

$$V_R = \frac{V_{DC}}{2fCR_L}$$ peak to peak Ripple Voltage

$$\text{Ripple Factor} = \frac{V_{RMS}}{V_{DC}} = \frac{\frac{V_R}{2\sqrt{3}}}{V_{DC}}$$

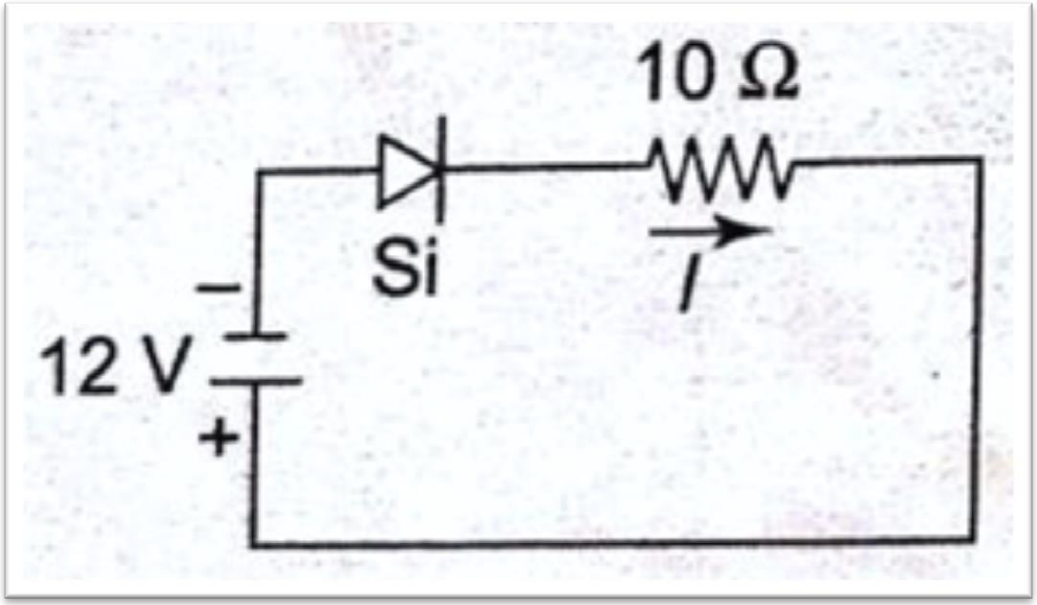
$$= \frac{V_{DC}}{V_{DC}\, 4\sqrt{3}\, fCR_L}$$

$$\textbf{Ripple Factor} = \frac{1}{4\sqrt{3}\, fCR_L}$$

PROBLEMS

For the given circuit's, find the value of *I*

Circuit 1

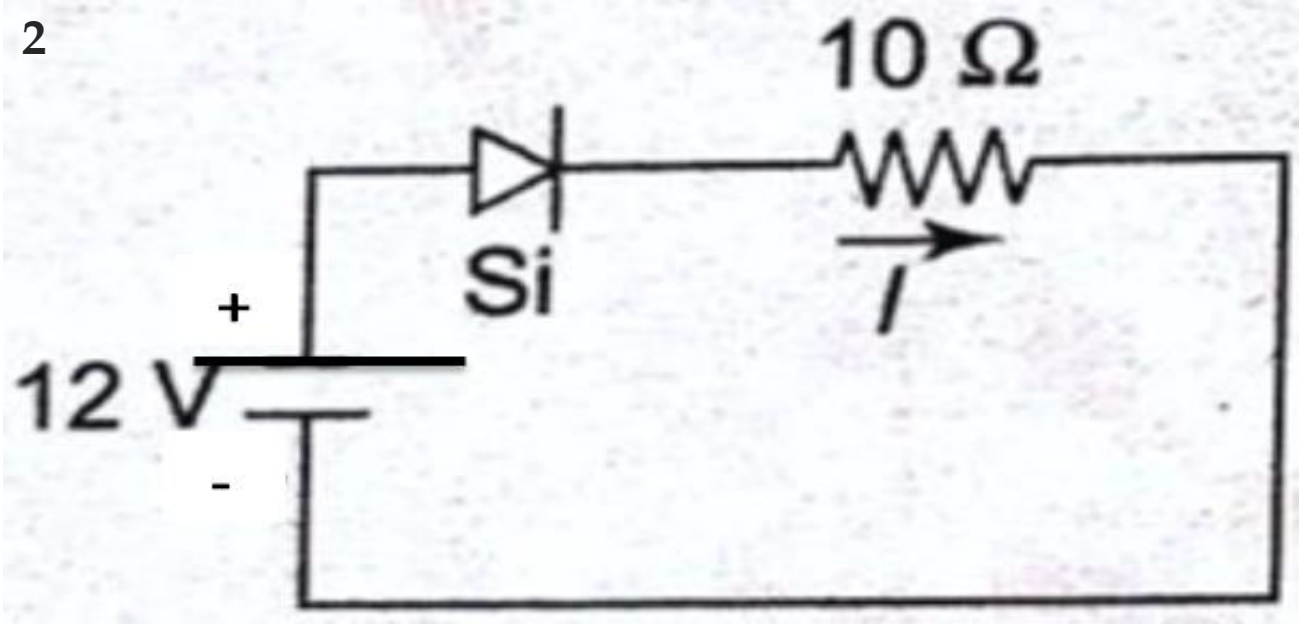


Since the diode gets Reverse biased, the Circuit becomes Open.

Hence there will be no flow of current in the circuit.

Hence I = 0A

Circuit 2



The given direction of the current is same as the circuit current (I_D). Hence we consider $I_D = I$

Applying KVL to the circuit, we get

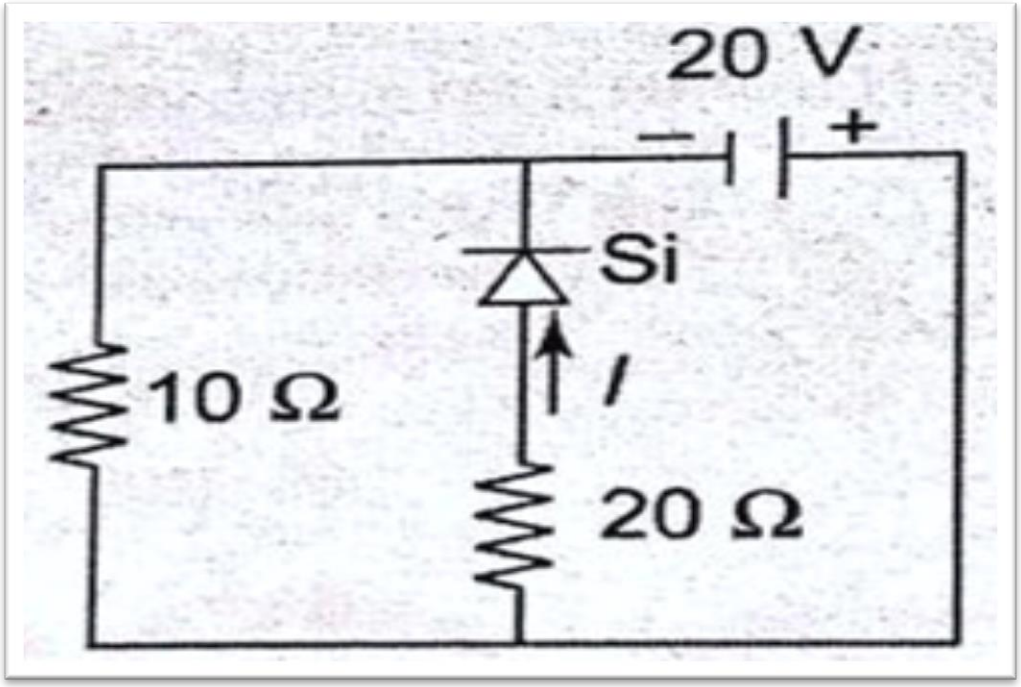
$$V_{IN} - V_D - V_R = 0$$

$$12 - 0.7 - I(10) = 0$$

$$I = (12 - 0.7) / 10$$

$$I = 1.13 \text{ A}$$

Circuit 3



The given direction of the current is same as the circuit current (I_D). Hence we consider $I_D = I$

Applying KVL to the circuit, we get

$$V_{IN} - V_R - V_D = 0$$

$$20 - I(20) - 0.7 = 0$$

$$I = (20 - 0.7)/20$$

$$I = \quad 0.965 \text{ A}$$

Circuit 4

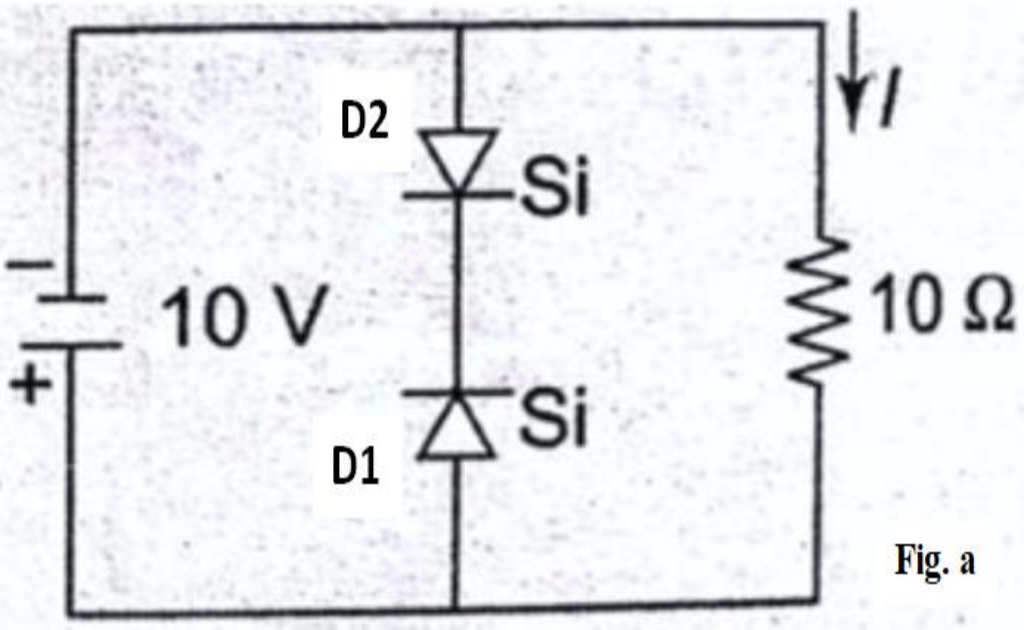


Fig. a

D1 gets forward biased, and D2 gets reverse biased.

Hence the total circuit reduces as shown in Fig. b

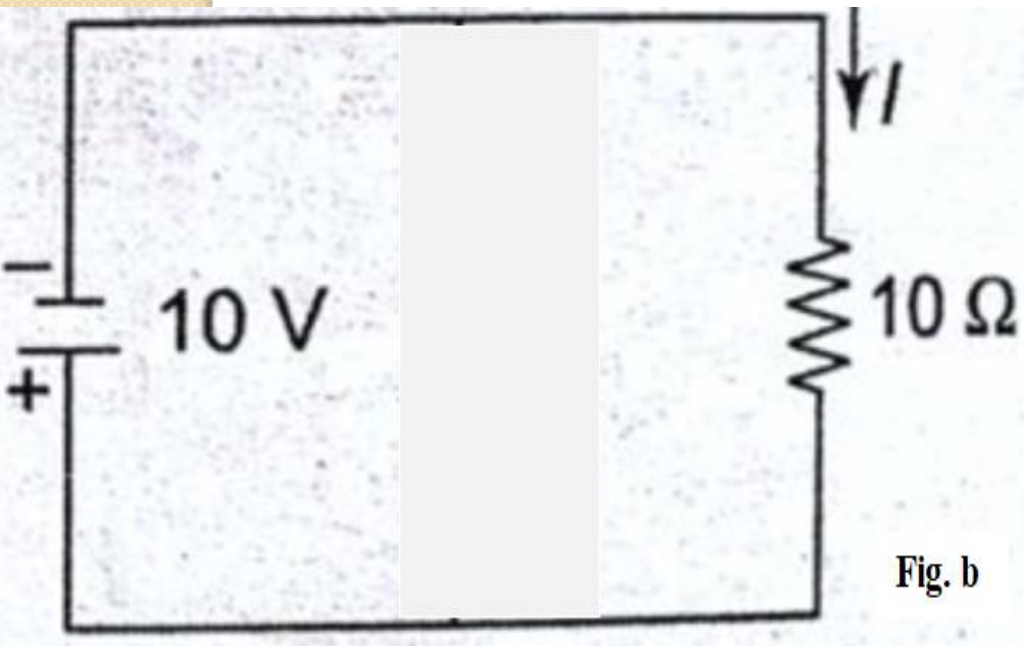


Fig. b

Now, by Applying KVL to the circuit in fig.b, we get,

$$10 = I_D * (10)$$

$$I_D = 10/10 = 1 \text{ A}$$

Since the direction of I is opposite to the flow of I_D. I will be equal to the value of I_D but negative value.

$$I = I_D = -1 \text{ A}$$

For the diode circuit, determine I_D and V_O, using approximate model of the diode.

Circuit 5

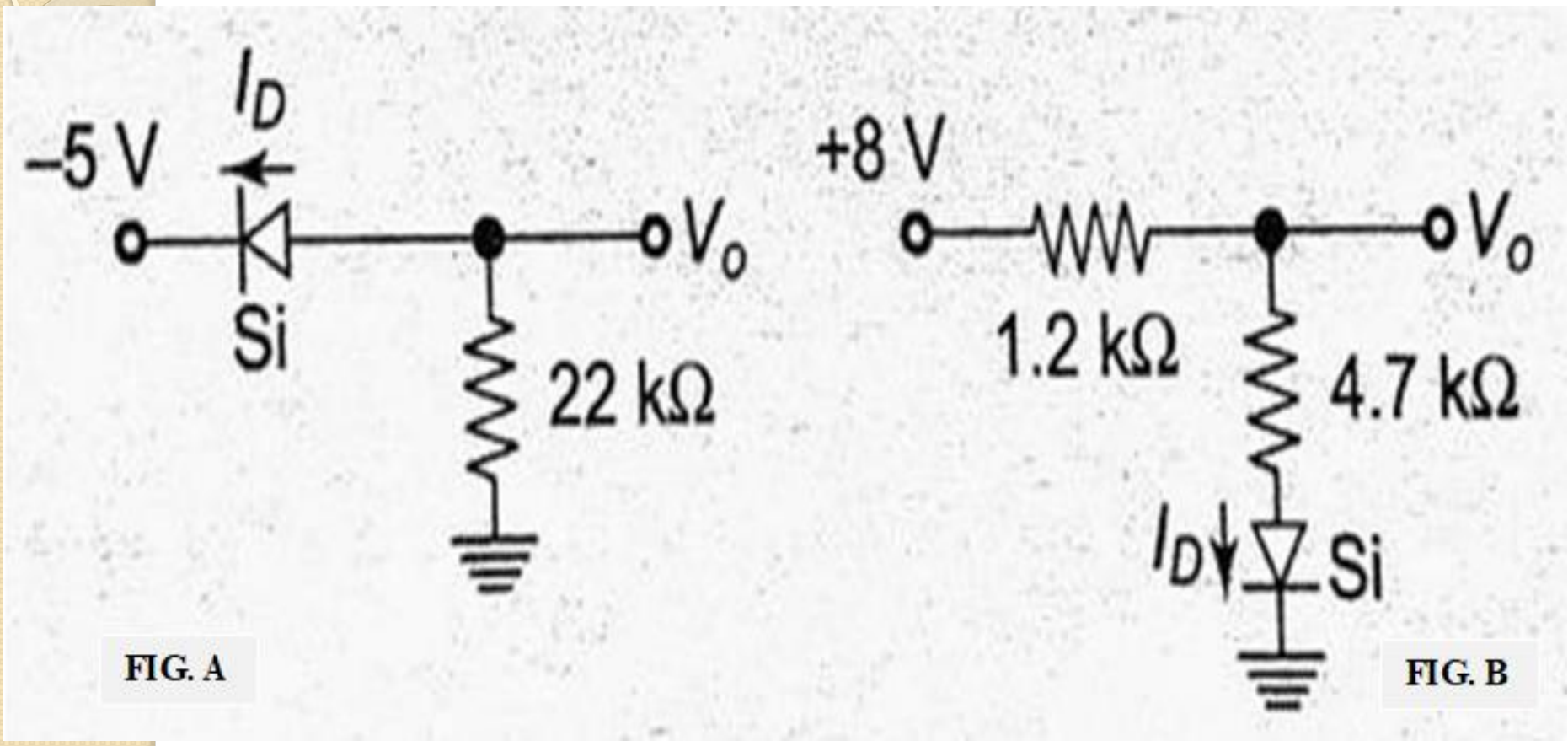


FIG. A

FIG. B

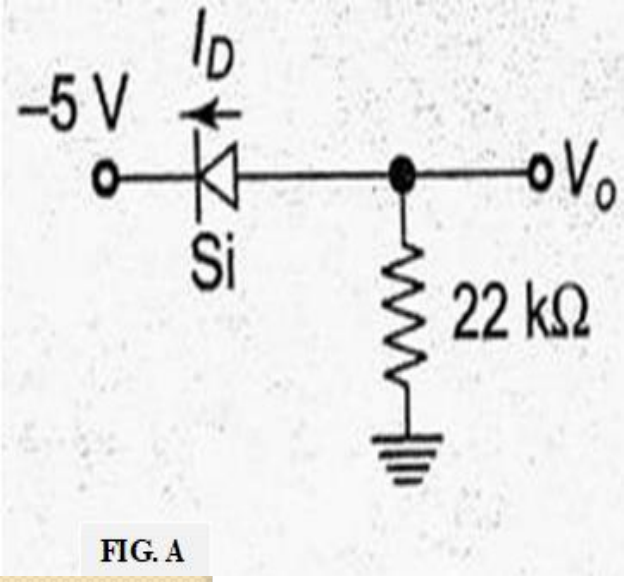
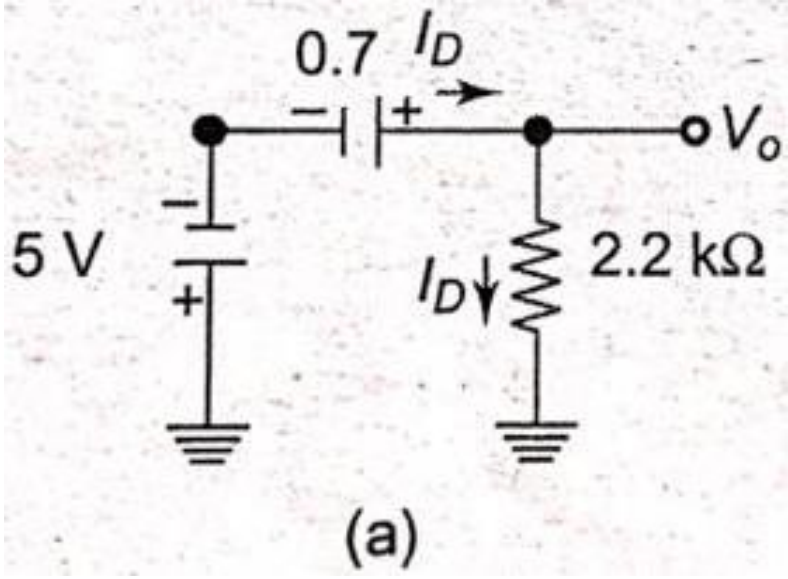


FIG. A

EQUIVALENT CIRCUIT



Applying KVL to the circuit, we get;

$$V_{IN} - V_R - V_D = 0$$

$$5 - (I_D * 22K) - 0.7 = 0$$

$$I_D = (5 - 0.7) / 22K$$

$$I_D = 0.195 \text{ mA}$$

$$V_O = V_R = I_D * R$$

$$V_O = 0.195m * 22K$$

$$V_O = 4.3V$$

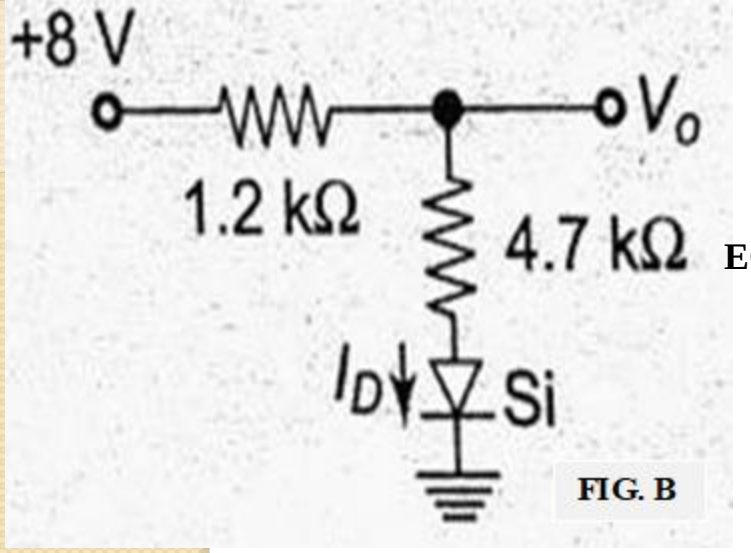
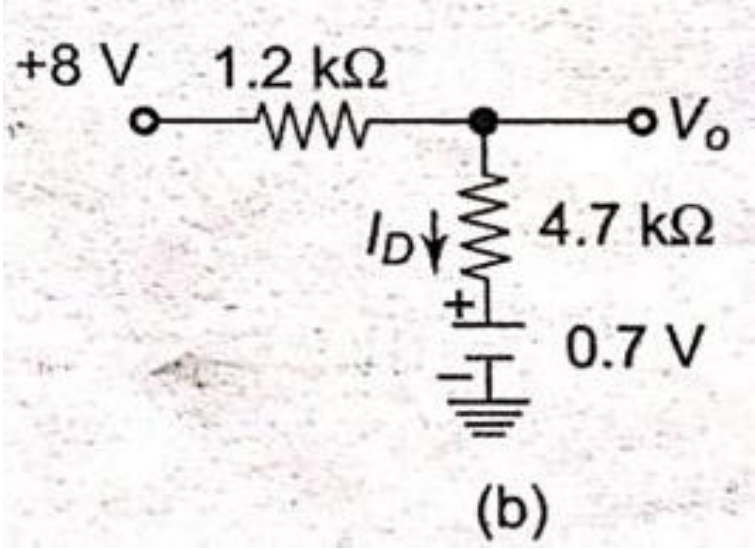


FIG. B

EQUIVALENT CIRCUIT



Applying KVL to the circuit, we get

$$V_{IN} - V_{R1} - V_{R2} - V_D = 0$$

$$8 - (I_D * R_1) - (I_D * R_2) - 0.7 = 0$$

$$I_D = (8\text{-}0.7) / (1.2K+4.7K)$$

$$I_D = 1.237\ mA$$

$$V_O = V_{in} - V_{R1} = V_{IN} - (I_D * R_1)$$

$$V_O = 8 - (1.237m*1.2K)$$

$$V_O = 6.5V$$

OR

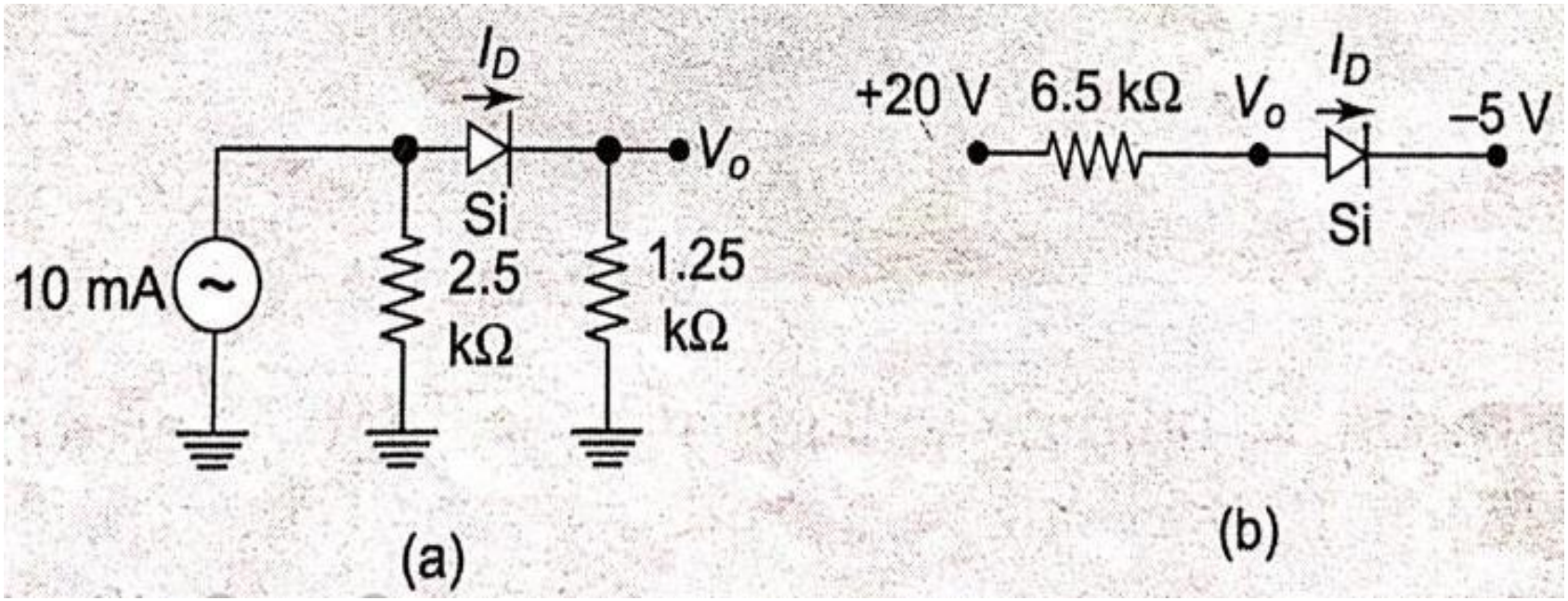
$$V_O = V_{R2} + V_D$$

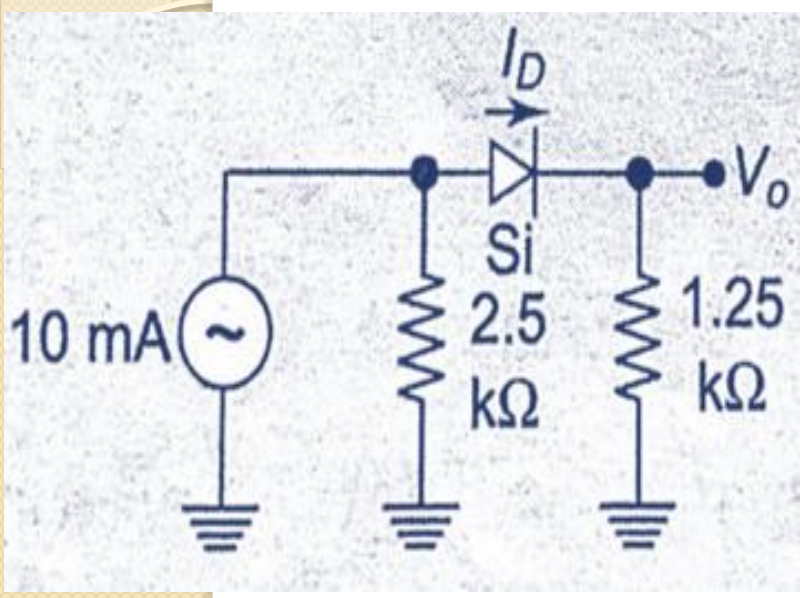
$$V_O = (1.237m*4.7K) + 0.7$$

$$V_O = 6.5V$$

Circuit 6

For the diode circuit, determine I_D and V_O, using approximate model of the diode.





Here, instead of Voltage source, they have given Current Source of 10mA and an Resistor of 2.5KΩ.

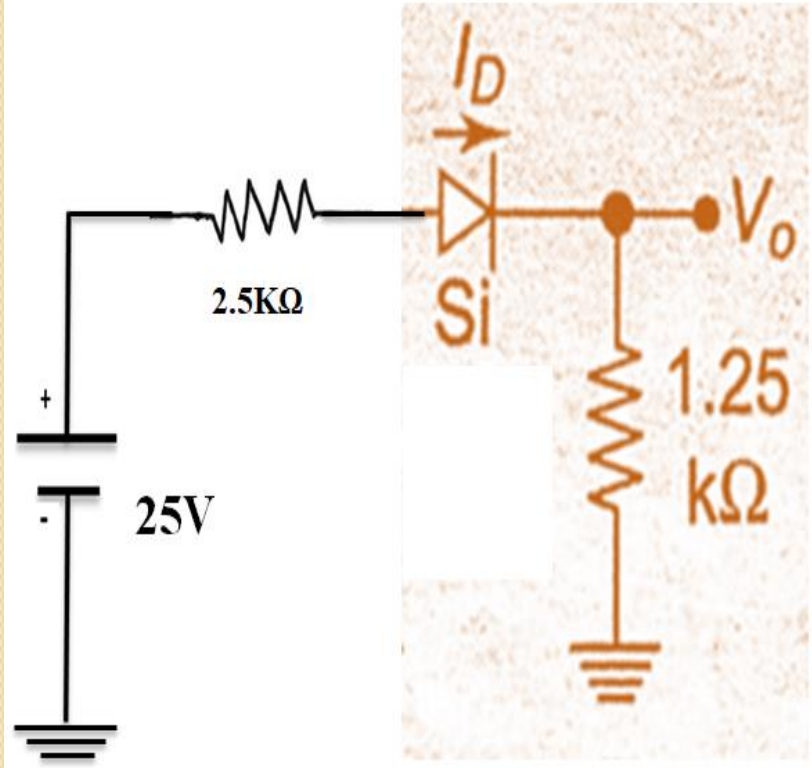
Now we are going to calculate the Voltage across 2.5KΩ resistor, by

$$V = I*R$$

$$V = 10m * 2.5K$$

$$V = 25V$$

The equivalent circuit is as shown below.



Now by Applying KVL to the circuit, we get

$$V_{IN} - V_{R1} - V_D - V_{R2} = 0$$

$$I_D = (V_{IN} - V_D) / (R_1 + R_2)$$

$$I_D = (25 - 0.7) / (2.5K + 1.25K)$$

$$I_D = 6.48 \text{ mA}$$

To find V_O

VIN – VR1 – VD – VO = 0 or VO – VR2 = 0

$V_O = V_{IN} - V_{R1} - V_D$

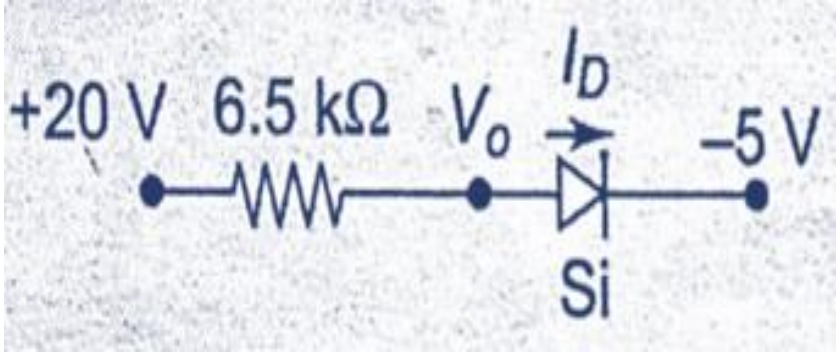
$V_O = 25 - (I_D * R1) - 0.7$

$V_O = 8.1V$

$V_O = V_{R2}$

$V_O = I_D * R_2$

$V_O = 8.1V$



Applying the KVLto the circuit

$$V_{IN1} - V_R - V_D + V_{IN2} = 0$$

$$20 - (I_D * 6.5K) - 0.7 + 5 = 0$$

$$I_D = (20 - 0.7 + 5)/6.5K$$

$$I_D = 3.78\ mA$$

$V_O = V_{IN1} - VR$

OR

$VIN2 - VO - VD = 0$

$V_O = 20 - (3.78m * 6.5K)$

$V_O = -4.3V$

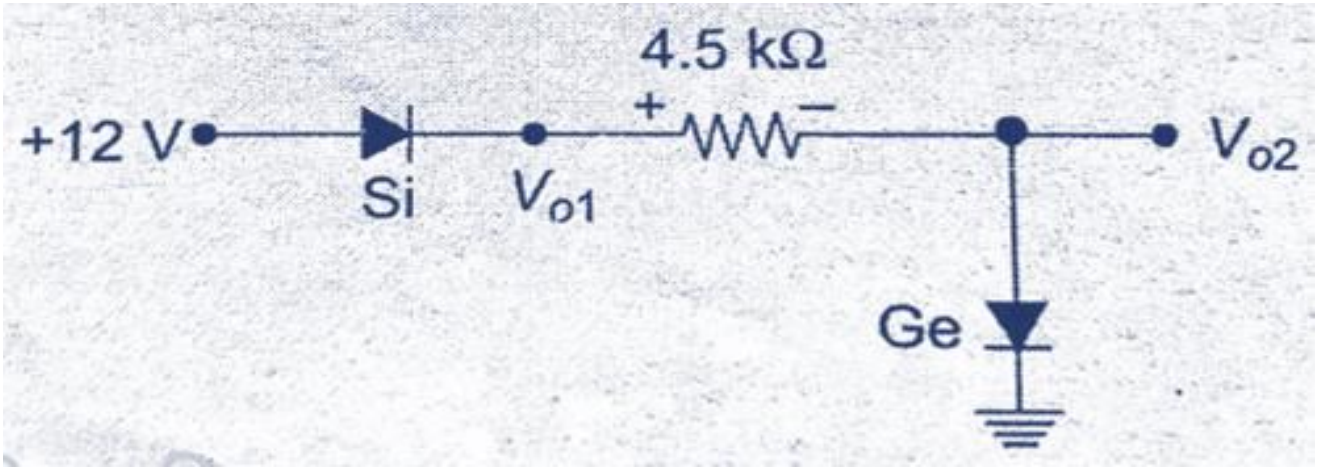
$V_O = -VIN2 + VD$

$V_O = -5 + 0.7$

$V_O = -4.3V$

Circuit 7

For the given circuit, determine V_{O1} and V_{O2}.



Applying KVL to the circuit, we get

$$V_{IN} - V_{Si} - V_{O1} = 0$$

$$V_{O1} = V_{IN} - V_{Si} = 12 - 0.7$$

$$V_{O1} = 11.3\ V$$

Applying KVL to the circuit, we get

$$V_{O2} = V_{Ge}$$

$$V_{O2} = 0.3V$$

OR

$$V_{O1} - V_{R1} - V_{O2} = 0$$

$$V_{O2} = V_{O1} - V_{R1}$$

$$V_{O2} = 0.32$$

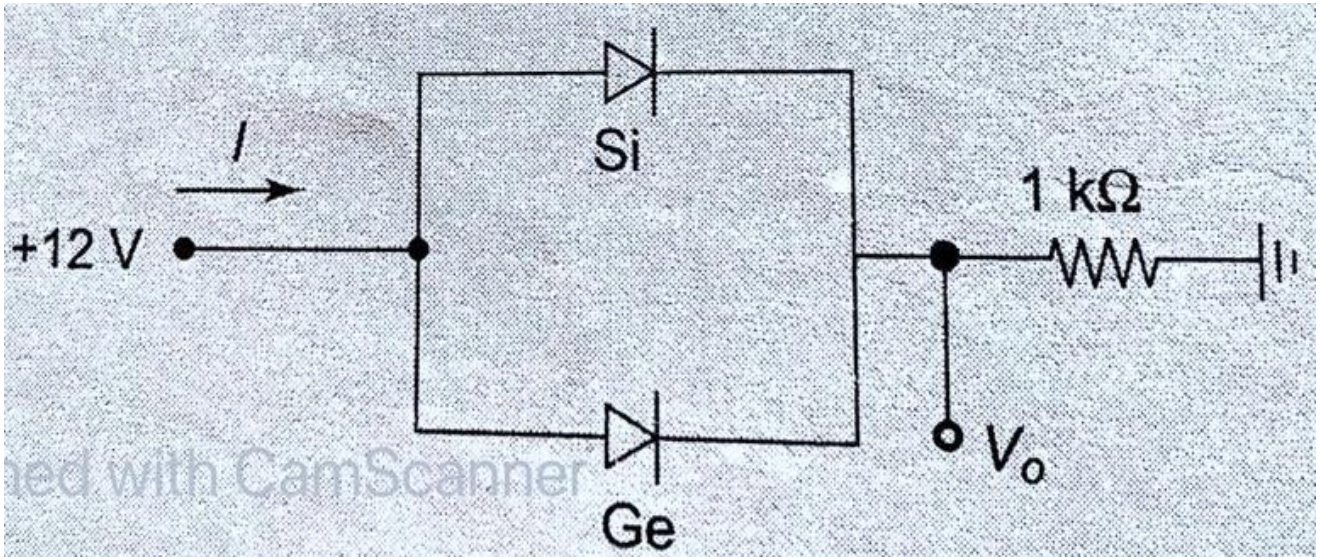
$$V_{O1} - V_{R1} - V_{Ge} = 0$$

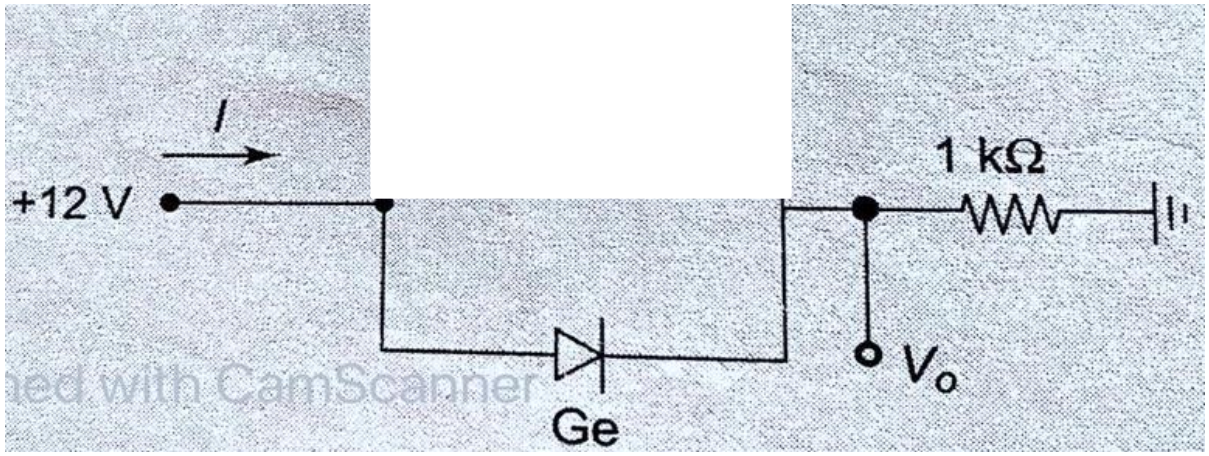
$$I_D = 11.3V - 0.3 / 4.5K$$

$$I_D = 2.44\ mA$$

For the given Circuit, determine V_O

Circuit 8





When the input voltage reaches 0.3V, immediately the Ge diode starts conducting, hence the Si diode will be in the OFF state. Hence the equivalent circuit is as shown above.

Now, By applying the KVL to the circuit, we get

$$V_{IN} - V_{Ge} - V_O = 0$$

$$V_O = 12 - 0.3$$

$$V_O = 11.7V$$

$$I_D = V_{IN} - V_{GE} / R$$

$$I_D = 11.7\ mA$$

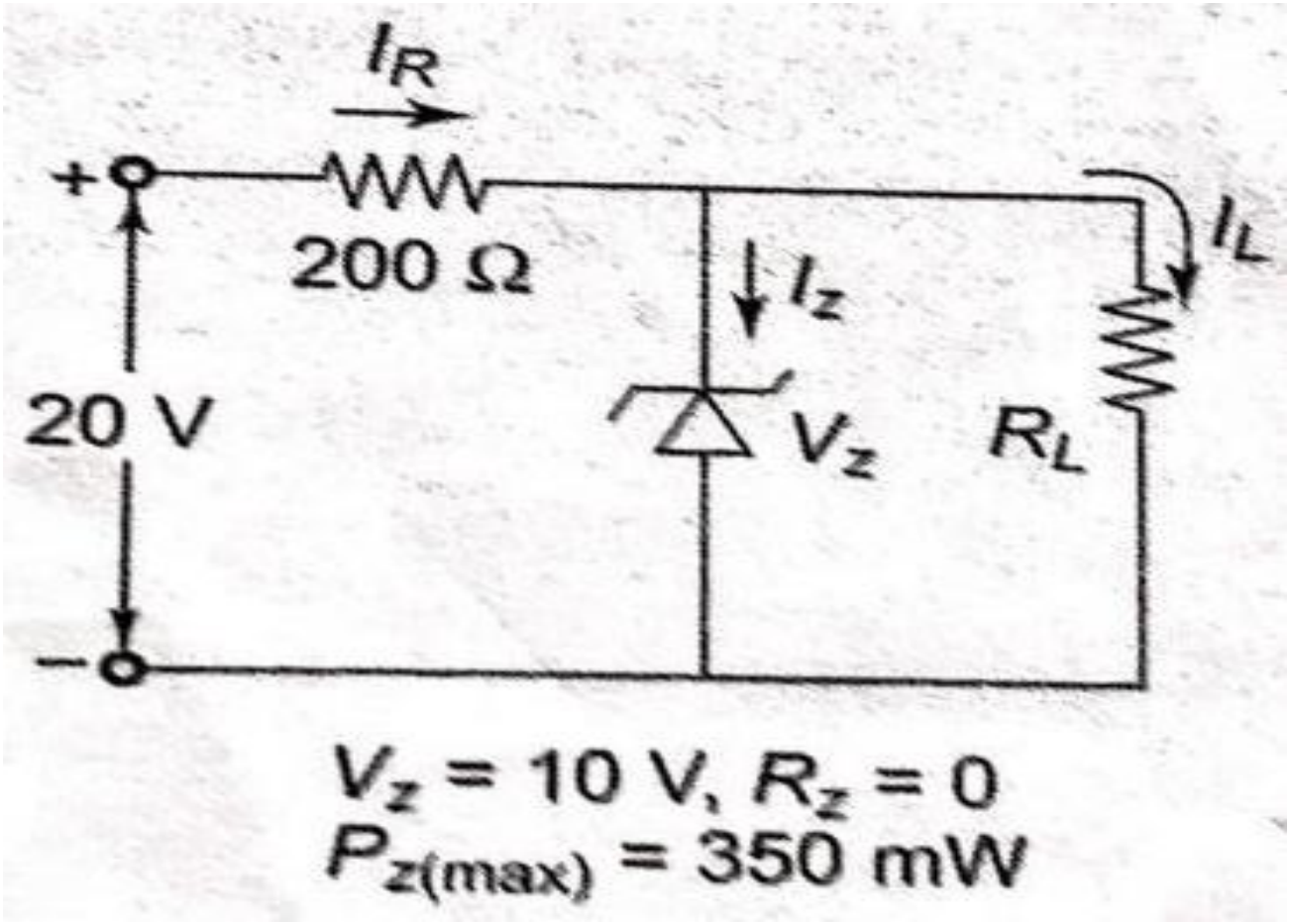
$$V_O = I*R$$

$$V_O = 11.7V$$

For the given Zener circuit;

1. For R_L = 180Ω, find all the Current and Voltages
2. Repeat 1 for R_L = 450Ω
3. Find the value of R_L for the zener to draw maximum power.
4. Find the minimum value R_L for the zener diode to be just in ON state.

Circuit 9



Assume the given R_L = 180 Ωis small, hence diode does not conducts,

$$\text{i.e } I_Z = 0$$

$$\text{Then } I_R = I_L = V_{IN} / (R+R_L)$$

$$I_R = I_L = 20 / (200+180) = 52.6\text{mA}$$

$$V_Z = V_L = I_L * R_L = 9.46\ \text{V} < 10\text{V}$$

Hence Assumption is Correct

FOR R_L = 450 Ω, We have to find, I_L, I_Z, I_R, V_L

Assume Zener conducts, $V_L = V_Z = 10\text{V}$

$$I_L = V_Z/R_L = 10 / 450 = 0.0222 = 22.22\text{mA}$$

$$I_R = (V_{IN} - V_Z)/ R = (20\text{-}10)/200 = 0.050 = 50\text{mA}$$

$$I_Z = I_R - I_L = (50 - 22.22)\ \text{mA} = 27.78\ \text{mA}$$

$$P_Z = V_Z * I_Z = 10*27.78\text{mA} = 277.8\ \text{mW}$$

$$P_Z < 350\ \text{mW (Given)}$$

When Zener draws maximum power, (i.e. I_Z is maximum, P_Z is fixed)

$$I_Z = P_Z/V_Z = 350m / 10 = 35mA$$

$$I_R = (V_{IN} - V_Z)/ R = (20\text{-}10)/200 = 0.050 = 50mA$$

$$I_L = I_R - I_Z = (50 - 35)mA = 15mA$$

$$R_L = V_L/I_L = V_Z/I_L = 10/15m = 667\ \Omega$$

Zener just in ON state (i.e $I_Z = 0$)

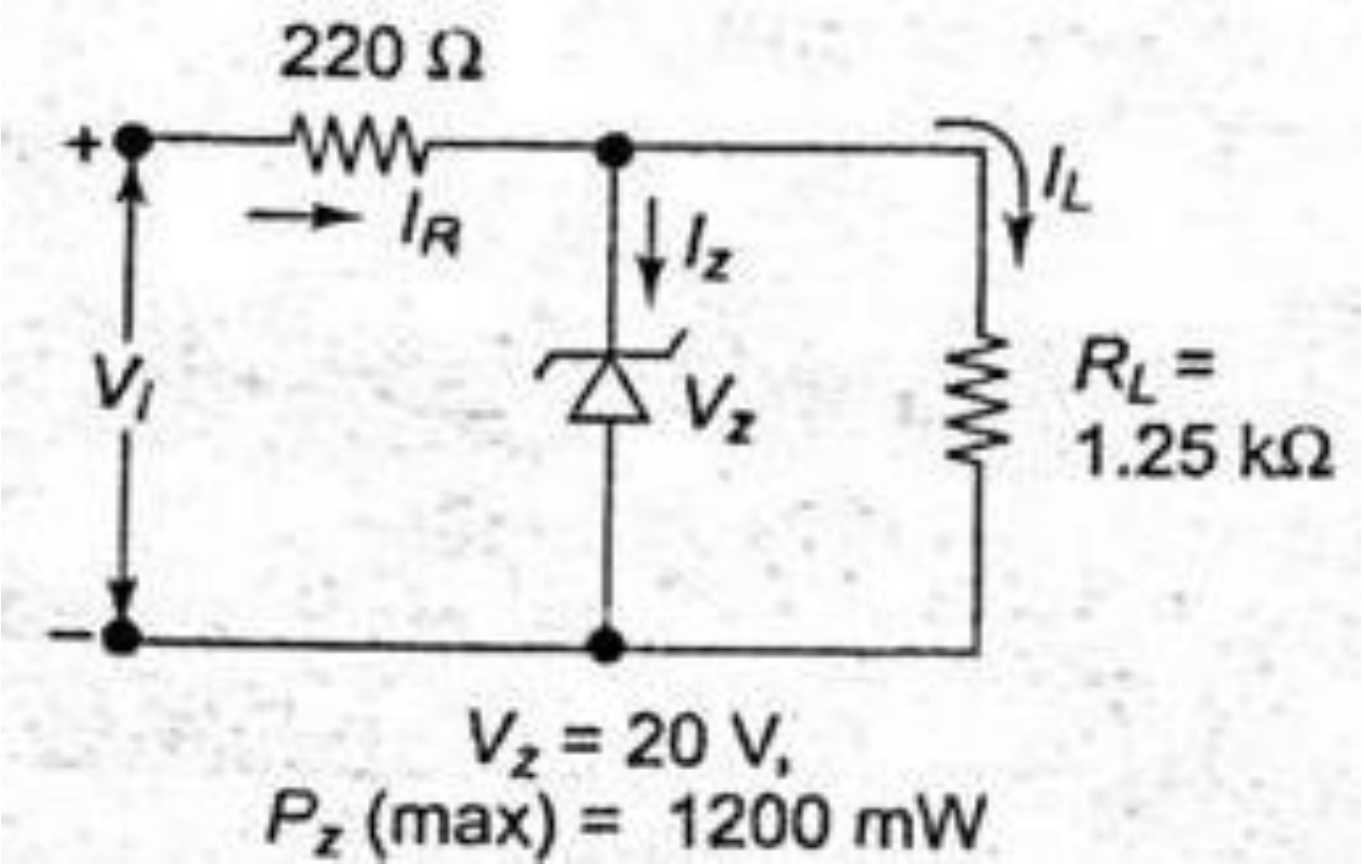
$$I_R = I_L = 50mA$$

$$V_L = V_Z = 10V$$

$$R_{L(min)} = V_L/I_L = 10/50m = 200\ \Omega$$

Determine the range of V_{IN} in which the Zener diode conducts

Circuit 10



To find the range of V_{IN} , we should calculate I_{Zmin} & I_{Zmax}

To find I_{Zmin} :

Zener diode is just in conducting state

$$I_Z = 0,\ V_Z = 20 \text{ (Given)}$$

$$I_R = I_L = V_Z / R_L = 20/1.25K = 16mA$$

$$V_{IN} = V_R + V_Z = (I_R * R) + 20 = (16m * 220) + 20$$

$$V_{IN} = 23.52V$$

To find I_{Zmax} :

$$I_{ZMAX} = P_Z/V_Z = 1200m/20 = 60mA$$

$$I_L = 16mA$$

$$I_R = I_{ZMAX} + I_L = 60m + 16m = 76mA$$

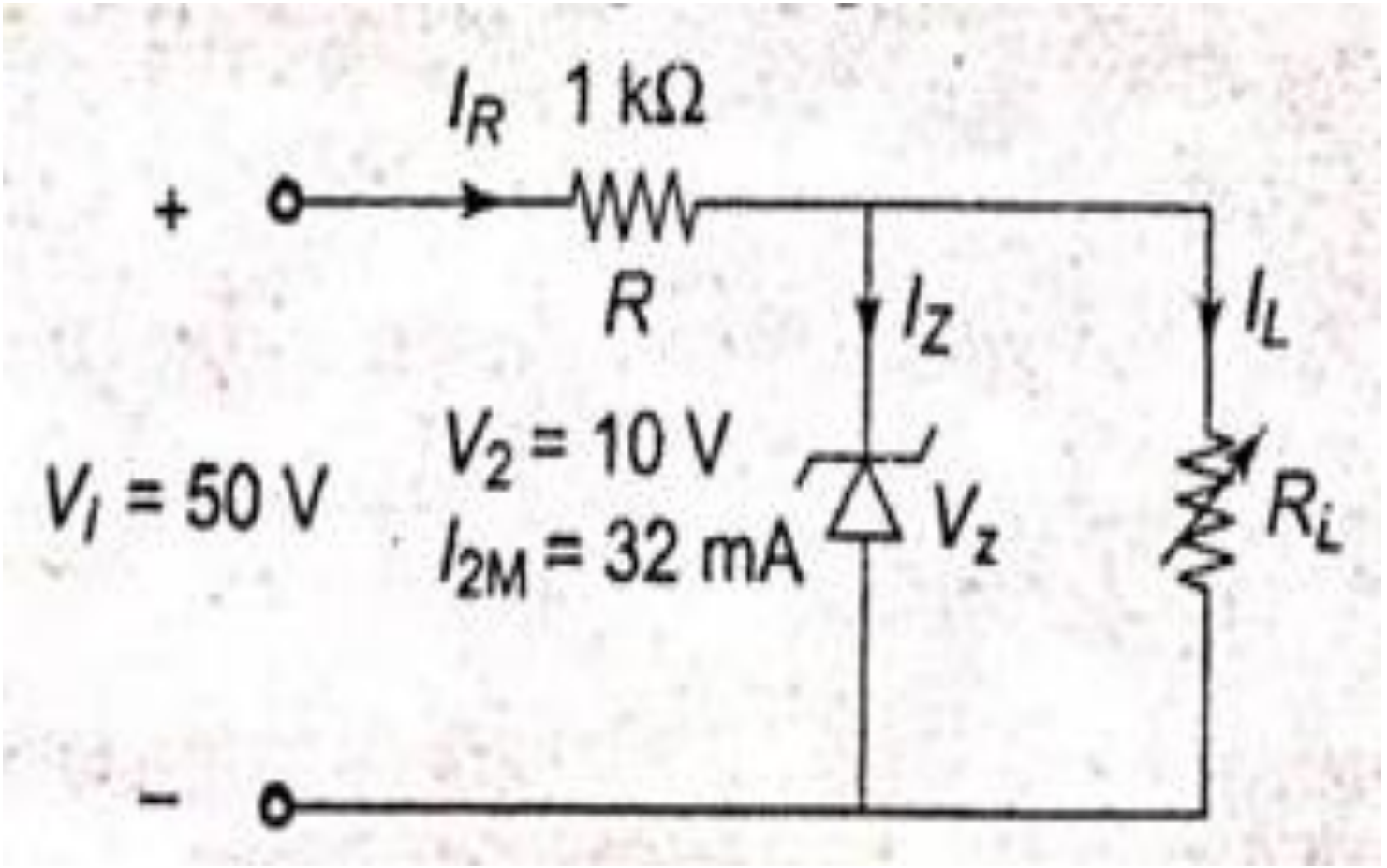
$$V_{IN} = V_R + V_Z = (I_R * R) + 20 = (76m * 220) + 20$$

$$V_{IN} = 36.72V$$

V_{IN} varies from 23.52 V to 36.72V to maintain constant load voltage V_L = 20V

For the circuit given, find the value of R_L & I_L that will result in V_L = 10V. Also determine the Wattage of diode.

Circuit 11



$$R_{LMIN} = R*VZ / (VIN – VZ)$$

$$R_{LMIN} = (1000*10) / (50 – 10)$$

$$R_{LMIN} = 250\ \Omega$$

$$I_R = (V_{IN} – V_Z)/ R = (50 – 10)/1000 = 40mA$$

$$I_{LMIN} = I_R – I_{ZMAX} = 40 – 32 = 8mA$$

$$R_{LMAX} = V_L/I_{LMIN} = 10/8m = 1.2k\Omega$$

$$P_{ZMAX} = V_Z*I_{ZMAX} = 10*32m = 320mW$$

Rectifier Equations:

To calculate V_{SRMS} Value:

$$\frac{N_1}{N_2} = \frac{V_P(RMS)}{V_S(RMS)}$$

(V_{PRMS} = Primary Voltage, N1 = Primary coil winding, N2 = Secondary coil winding)

To calculate V_M:

$V_M = 2*V_{SRMS}$ (Half Wave) ; $V_M = \sqrt{2} *V_{SRMS}$ (Full Wave)

To calculate [V_{DC} or (V_L)]:

$\mathbf{V_{DC} = V_M/\pi}$ (HW) ; $\mathbf{V_{DC} = 2V_M/\pi}$ (FW)

$\mathbf{V_{DC} = I_{DC}*R_L}$ (Both Full Wave & Half Wave)

To calculate %Regulation: $\%\text{Regulation} = \frac{V_{NL}-V_{FL}}{V_{FL}} \times 100$

V_{NL} = No Load Voltage; $\mathbf{V_M/\pi}$ **for HW ;** $\mathbf{2V_M/\pi}$ **for FW**

V_{FL} = Full Load Voltage $\mathbf{I_{DC}R_L}$ **for HW & FW**

To calculate I_M:

$$I_m = \frac{V_m}{R_s + R_f + R_L}$$

(R_S= Secondary Resistance, R_F= Forward resistance of Diode, R_L= Load Resistance)

To calculate I_{RMS}:

$I_{RMS} = I_M/2$ (Half Wave); $I_{RMS} = I_M/\sqrt{2}$ (Full Wave)

To calculate I_{DC}:

$I_{DC} = I_M/\pi$ (HW); $I_{DC} = 2I_M/\pi$ (FW)

To calculate I_{AVG}:

$I_{AVG} = I_{DC}$

To calculate P_{DC} *(DC Power)**:*** $P_{DC} = V_{DC} * I_{DC} = (I_{DC})^2 * R_L$

To calculate P_{DC} *(AC Power)**:*** $P_{AC} = (I_{RMS})^2 *$ Total Resistance

$P_{AC} = (I_{RMS})^2 * (R_S + R_F + R_L)$

To calculate **η*:*** $\eta = \frac{P_{DC}}{P_{AC}}$ $\eta = \frac{(IDC)2 * RL}{(IRMS)^2 * (RS+RF+RL)}$

$\% \eta = \frac{P_{DC}}{P_{AC}} * 100$; $\% \eta = \frac{(IDC)2 * RL}{(IRMS)^2 * (RS+RF+RL)} * 100$

To calculate **γ** *(without Filter)**:***

$$\gamma = \sqrt{\frac{V_{L\,rms}^2}{V_{L\,dc}^2} - 1}$$ (For HW & FW),

Conclude after calculating it by the Constant Values of HW & FW Rectifiers;

i.e. **γ= 1.21** for HW & **γ = 0.485** for FW

To calculate **γ** *(with Filter)**:***

$\gamma = \frac{1}{2\sqrt{3}\,fCR_L}$ (for HW with C filter) $\gamma = \frac{1}{4\sqrt{3}\,fCR_L}$ (for FW with C filter)

1

A half wave rectifier circuit is supplied from a 230v, 50Hz supply with a step down ratio of 3:1 to a resistive load of 10KΩ. The diode forward resistance is 75Ω while transformer secondary resistance is 10Ω. Calculate maximum, average, RMS values of current, DC output voltage, efficiency of rectification and ripple factor.

Given:

R_L = 10KΩ , R_f = 75Ω , R_S = 10Ω , N1 = 3, N2 = 1, $V_{P(RMS)}$ = 230V,

The given supply voltages are always r.m.s values. $V_{P(RMS)}$=230v,

$$\frac{N_1}{N_2} = \frac{V_P(RMS)}{V_S(RMS)} \quad ; \quad \frac{N_1}{N_2} = \frac{3}{1}$$

$$\frac{N_2}{N_1} = \frac{V_S(RMS)}{V_P(RMS)}$$

$$\frac{1}{3} = \frac{V_S(RMS)}{230}$$

$$V_S(RMS) = 76.667V$$

To Find: $\mathbf{I_M, I_{DC}, I_{RMS}, V_{DC}, \eta, \gamma}$

$$V_m = 2 * V_S\,(RMS) = 2\,X\,76.667$$

$$\boldsymbol{V_m = 153.334V}$$

$$I_m = \frac{V_m}{R_s + R_f + R_L} = \frac{153.33V}{10 + 75 + 10 \times 10^3}$$

$$\boldsymbol{I_m = 15.2mA}$$

$$I_{av} = I_{DC} = \frac{I_m}{\pi} = \frac{15.2}{\pi} = \boldsymbol{4.83mA}$$

$$I_{rms} = \frac{I_m}{2} = \frac{15.2}{2} = \boldsymbol{7.6mA}$$

$$V_{DC} = dc\ output\ voltage = I_{DC}R_L = \mathbf{48.3V}$$

$$P_{DC} = dc\ output\ power = V_{DC} * I_{DC} = \mathbf{0.233W}$$

This can also be obtained as,

$$P_{DC} = {I_{DC}}^2 R_L = \left(\frac{I_m}{\pi}\right)^2 R_L = \mathbf{0.233W}$$

$$P_{AC} = ac\ input\ power = {I_{rms}}^2 \left[R_s + R_f + R_L\right] = 0.582W$$

$$\%\,\eta = \frac{P_{DC}}{P_{AC}} \times 100 = \mathbf{40.24\%}$$

The ripple factor is constant for half wave rectifier and is 1.21

$$\boldsymbol{\gamma = 1.21}$$

2 A half wave rectifier with R_L=1KΩ is given an input of 10V peak from step down transformer. Calculate D.C voltage and load current for ideal and silicon diode.

Given:

R_L=1KΩ

V_m= 10V (Peak Value is the maximum Value)

Case 1: Ideal Diode

V_T = 0 V, R_f = 0Ω

$$V_{DC} = \frac{V_m}{\pi} = \frac{10}{\pi} = 3.18V$$

$$I_L = I_{DC} = \frac{V_{DC}}{R_L} = 3.18mA$$

Case 2: Silicon Diode

V_T = 0.7 V , R_f = 0Ω

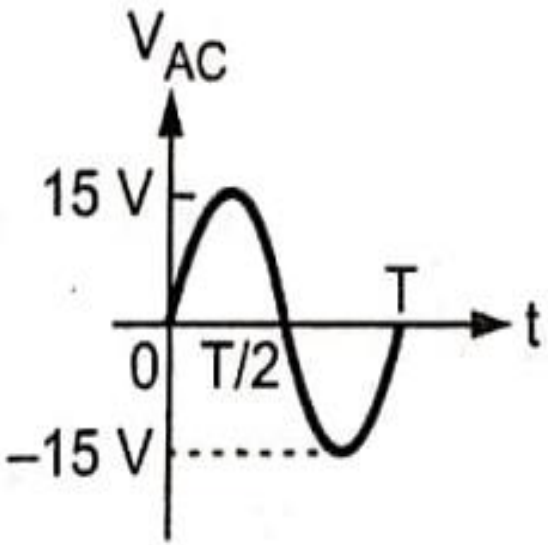
$$V_{DC} = \frac{V_m - V_T}{\pi} = \frac{10 - 0.7}{\pi} = 2.96V$$

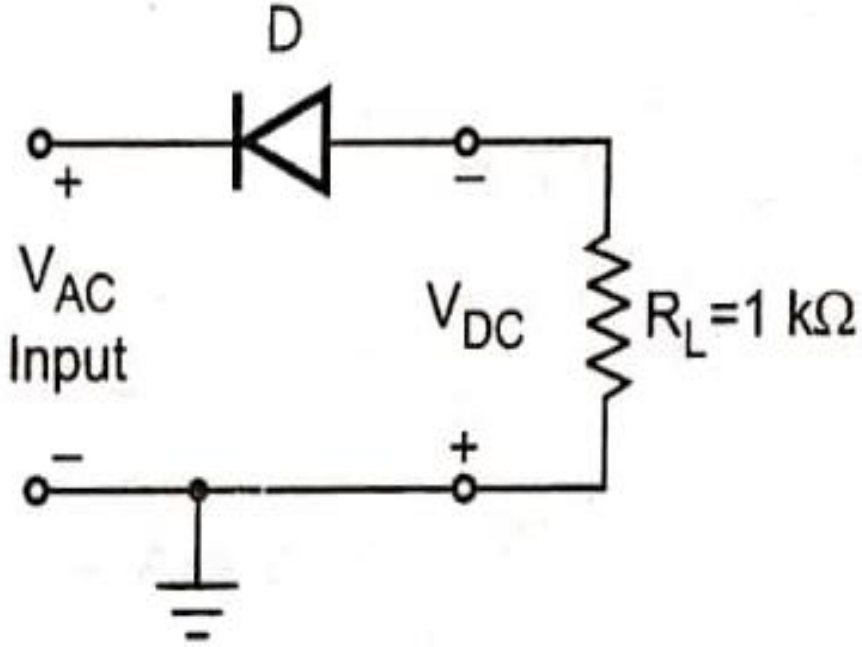
$$I_{DC} = \frac{V_{DC}}{R_L} = 2.96mA$$

3

a) Assuming ideal diode, calculate the d.c. output voltage for the network shown in the figure 1.

b) Repeat part (a) if the ideal diode is replaced by a silicon diode, having a cut-in voltage of 0.7V. Neglect diode forward-resistance.



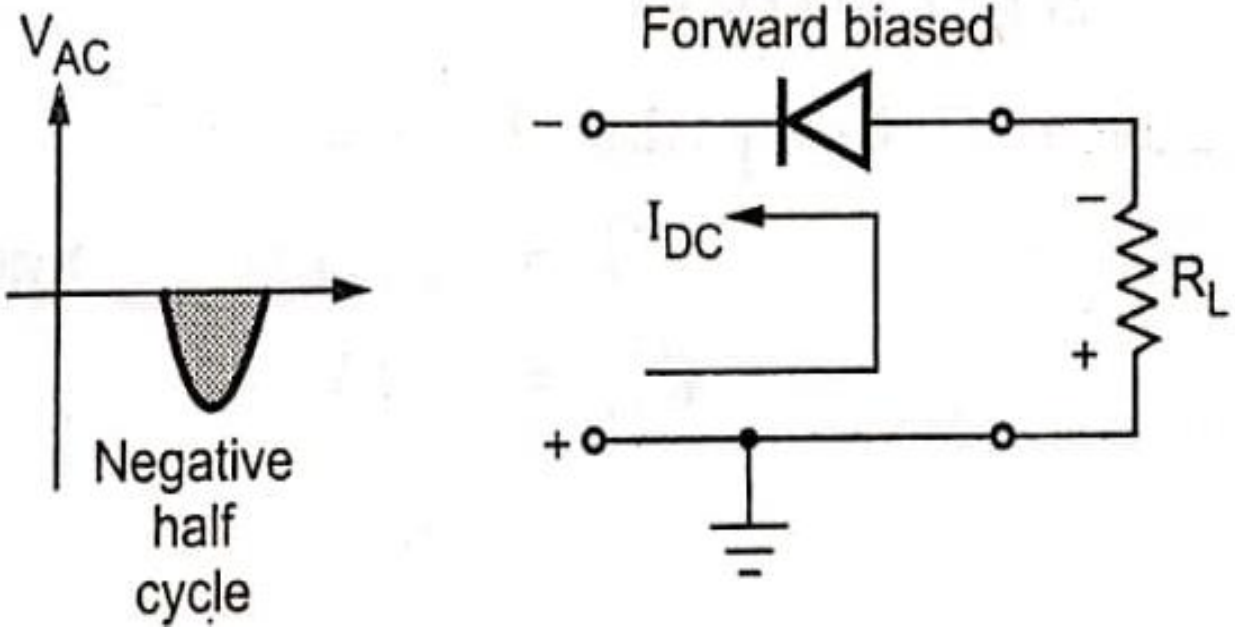


Given:

R_L = 1KΩ , V_M = 15V

i. For ideal diode ; VDC = ?

ii. For Silicon Diode; VDC = ?



The circuit conducts for Negative Half Cycle ***(∵ Diode gets forward biased)***.

Hence, we get negative output (i.e Negative Voltage)

For Ideal Diode:

$$\text{D. C. output voltage} = \frac{-\text{Maximum value of a. c. input voltage}}{\pi}$$

$$V_{DC} = \frac{-V_M}{\pi}$$

$$V_{DC} = \frac{-15}{\pi}$$

$$\boldsymbol{V_{DC} = -4.77\ V}$$

For Silicon Diode:

$$V_{DC} = \frac{-[VM - VT]}{\pi}$$

$$V_{DC} = \frac{-[15 - 0.7]}{\pi}$$

$$\boldsymbol{V_{DC} = -4.55\ V}$$

4

In a half wave rectifier, the input is 300 sin 314t. Find its average output voltage.

Comparing the input with standard input equation:

$$\mathbf{V_{IN} = V_{AC} = V_m \sin \omega t}$$

$$\mathbf{V_{IN} = V_{AC} = 300 \sin 314t}$$

$\therefore$ V_m=300V , $\boldsymbol{\omega} = 2 * \pi * f = 314$

Therefore, Average output voltage is,

$$V_{DC} = \frac{V_m}{\pi} = \frac{300}{\pi} = 95.4929V$$

5

A full wave rectifier circuit is fed from a transformer having a center-tapped secondary winding. The rms voltage from either end of secondary to center tap is 30V. If the diode forward resistance is 2Ω and that of the half secondary is 8Ω, for a load of 1KΩ, calculate.

i. Power delivered to load, ii.% Regulation at full load iii.Efficiency of rectification

Given:

V_s=30V, R_f =2Ω, R_s=8Ω, R_L=1K Ω

P_{DC} = ?, %Regulatipn = ?, η = ?

$$V_s = V_{RMS} = 30V$$

$$V_m = V_s\sqrt{2} = 30\sqrt{2} = 42.426V$$

$$I_m = \frac{V_m}{R_f + R_L + R_s} = \frac{30\sqrt{2} =}{2 + 1000 + 8} = 42mA$$

$$I_{DC} = \frac{2}{\pi} I_m = 26.74mA$$

1. Power delivered to the load $= P_{DC} = I_{DC}^{2} R_L$

$$P_{DC} = (26.74 \times 10^{-3})^2 (1K\Omega)$$

$$\underline{= 0.715W}$$

2. $\%Regulation = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100$

$V_{NL} = V_{DC\ No\ Load} = \frac{2}{\pi} V_m = \frac{2}{\pi} 30\sqrt{2} = 27V$

$V_{FL} = V_{DC\ Full\ Load} = I_{DC} R_L = \left((26.74 \times 10^{-3})(1K\Omega)\right) = 26.74V$

$$\%Regulation = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100 = \frac{27 - 26.74}{26.74} \times 100$$

$$\underline{\%Regulation = 0.97\%}$$

3. Efficiency of Rectification, $\eta = \frac{D.C.\ Output}{A.C.\ input}$

$$\eta = \frac{I_{dc}^2 * R_L}{I_{rms}^2 * R_L} = \left(\frac{I_{dc}}{I_{rms}}\right)^2$$

$$\eta = \left(\frac{2I_m/\pi}{I_m/\sqrt{2}}\right)^2$$

$$\eta = 0.802$$

$$\%\eta = \quad 0.802 \text{ X}100$$

$$\%\eta = \quad 80.2\ \%$$

6

A full wave rectifier uses a diode with forward resistance of 1Ω. The Transformer secondary is center tapped with output 10-0-10 V_{RMS} and has resistance of 5Ω for each half section. Calculate

i. No-load voltage, ii. D C output voltage at 100mA, iii. % Regulation at 100mA

Given:

$R_f = 1\Omega$, $R_s = 5\Omega$, $V_{s(rms)} = 10V$,

i. V_{NL} =?, ii. V_{DC} =? at I_{DC} = 100mA, iii. %Regulation = ? at I_{DC} = 100mA

$$\boldsymbol{V_M = V_{SRMS} * \sqrt{2} = 1401421V}$$

i. $$V_{DC}(\text{no load}) = \frac{2V_m}{\pi} = 2 \times \frac{14.1421}{\pi}$$

$$\boldsymbol{V_{DC}(no\ load) = 9.0031V}$$

ii. $$V_{DC} = V_{DC}(\text{full load}) = I_{DC} * R_L$$

Since R_L is unknown, we have to find R_L

$$I_{DC} = 100\text{mA} = \frac{2}{\pi} I_m$$

$$I_m = \frac{\pi \times 100\text{mA}}{2} = 157.079\text{mA}$$

But,

$$I_m = \frac{V_m}{R_f + R_s + R_L}$$

$$157.079 \times 10^{-3} = \frac{14.1421}{1 + 5 + R_L}$$

$$R_L = 84.0317\Omega$$

$$V_{DC} = I_{DC}R_L = 100 \times 10^{-3} \times 84.0317$$

$$\boldsymbol{V_{DC} = 8.4031V}$$

iii.

$$\%\text{Regulation} = \frac{V_{dc}(\text{no load}) - V_{dc}(\text{full load})}{V_{dc}(\text{full load})}$$

$$= \frac{9.0031 - 8.4031}{8.4031} \times 100$$

$$= 7.14\%$$

7

What is the necessary A.C. input power from the transformer secondary used in a half wave rectified to deliver 500W of D.C. power to the load? What would be the A.C. input power for the same load in a full wave rectifier?

Given: P_{DC}=500W, Half wave rectifier

For half wave rectifier, $\%\eta = 40.5\%$

$$\%\eta = \left[\frac{P_{DC}}{P_{AC}}\right]*100$$

$$40.5 = \left[\frac{500}{P_{AC}}\right]*100$$

$$P_{AC} = \left[\frac{500}{40.5}\right]*100$$

$$\boldsymbol{P_{AC} = 1234.567W}$$

For half wave rectifier, $\%\eta = 81\%$

$$\%\eta = \left[\frac{P_{DC}}{P_{AC}}\right]*100$$

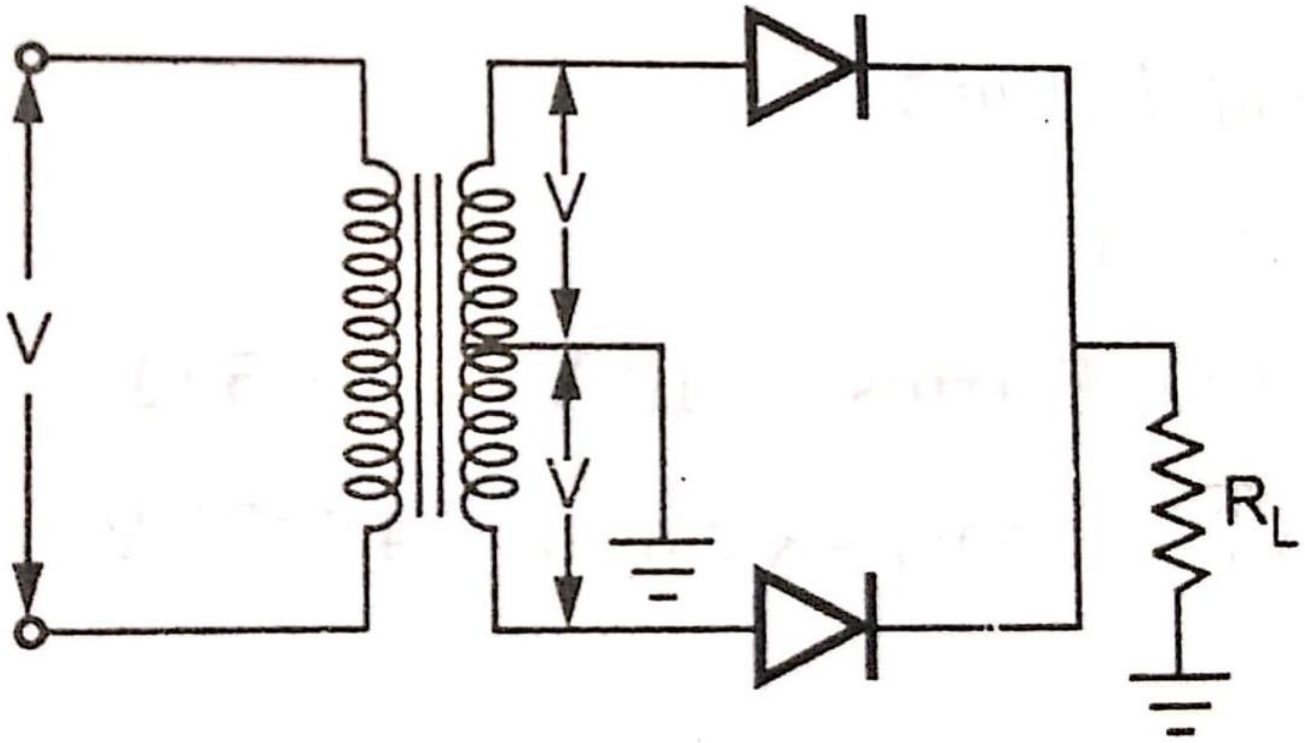
$$81 = \left[\frac{500}{P_{AC}}\right]*100$$

$$P_{AC} = \left[\frac{500}{81}\right]*100$$

$$\boldsymbol{P_{AC} = 617.284W}$$

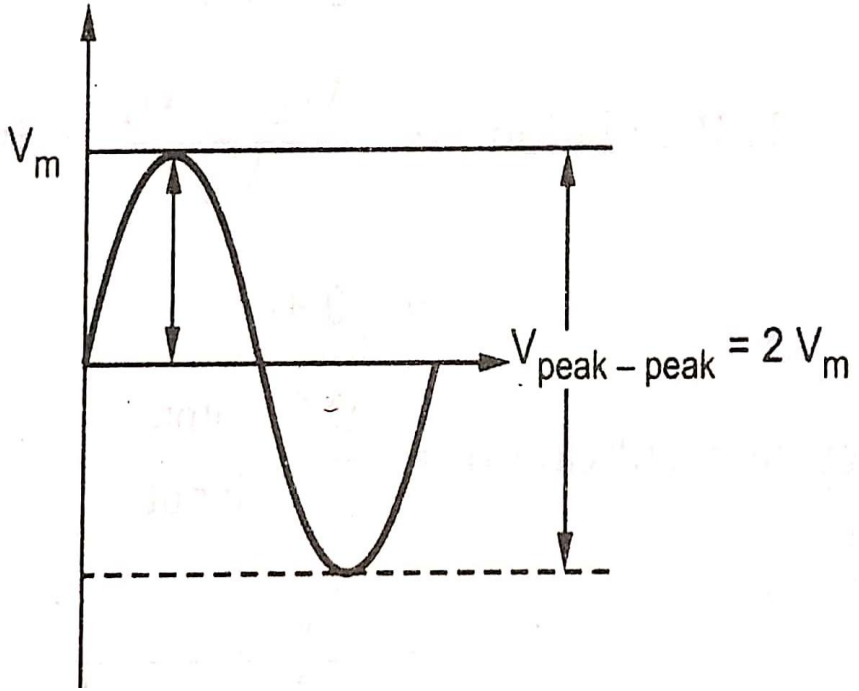
8

For the full-wave rectifier circuit shown in the Fig, V is a sinusoidal voltage & R_L =100Ω. If the maximum allowable average DC current in each diode is 1A. Calculate the maximum allowable peak-to-peak value of V. Assume two diode to be identical and neglect diode resistance in forward direction.



Given: $R_L = 100\Omega$, $V_{AC} = V$

Let V_m is maximum value or amplitude of sinusoidal voltage, across each half of the secondary winding.



Maximum I_{DC} for each diode=1A, i.e. $I_{DC} = 1A$

A full wave rectifier essentially consists of two independent half wave rectifiers feeding a common load.

The average I_{DC} per Half wave rectifier diode

$$I_{DC} = \frac{I_m}{\pi} = \frac{V_m}{\pi R_L}$$

$$\text{where } I_m = \frac{V_m}{R_L} \text{ as } R_f = 0, R_S = 0$$

$$1A = \frac{V_m}{\pi R_L}$$

$$V_m = \pi R_L = \pi \times 100$$

$$V_m = 314.16V$$

$$V_{\text{peak to peak}} = V_{max} \times 2 = 628.32V$$

9

In a full wave rectifier the input is from a 30-0-30V transformer. The load and diode forward resistance are 100Ω and 10Ω respectively. Calculate the average voltage and efficiency.

Given:

$R_f = 10\Omega$, $R_L = 100\Omega$, $V_{SRMS} = 30V$, $I_{AV} = I_{DC} = ?$, $\eta = ?$

$$V_M = \sqrt{2} * V_{RMS} = \sqrt{2} * 30 = 42.426V$$

$$I_m = \frac{V_m}{R_f + R_L} = \frac{42.4264}{100 + 10} = 0.3856A$$

$$I_{DC} = \frac{2I_m}{\pi} = \frac{2 \times 0.3856}{\pi} = 0.2455A$$

$$V_{DC} = I_{DC} R_L = 0.2455 \times 100 = 24.55\ V$$

$$P_{DC} = {I_{DC}}^2 R_L = 6.027\ \text{W}$$

$$P_{AC} = {I_{RMS}}^2 (R_f + R_L) = \left(\frac{I_m}{\sqrt{2}}\right)^2 (R_f + R_L) = 8.1778\ W$$

$$\%\eta = \frac{P_{DC}}{P_{AC}} \times 100 = \frac{6.027}{8.1778} \times 100 = 73.69\%$$

10

In a two diode F.W.R (Full wave rectifier) circuit, the voltage across each half of the transformer secondary is 100V. The load resistance is 950Ω and each diode has a forward resistance of 50Ω. Find the load current and the rms value of the input current.

Given:

$V_{S\,RMS}$=100V, R_f =50Ω, R_L = 950Ω, I_L =?, I_{RMS} = ?

$$V_M = \sqrt{2}V_{S\,RMS} = \sqrt{2} \times 100 = 141.42V$$

$$I_M = \frac{V_M}{R_S + R_f + R_L} = \frac{141.42}{0 + 50 + 950} = 0.141\ A$$

$$I_{RMS} = \frac{I_m}{\sqrt{2}} = \frac{0.141}{\sqrt{2}} = 0.0997A$$

$$\boldsymbol{I_{RMS} = 99.7mA}$$

$$I_{DC} = \frac{2I_M}{\pi} = \frac{2 \times 0.141}{\pi} = 0.0897A$$

$$\boldsymbol{I_{DC} = 89.7mA}$$

THANK YOU

MODULE 2

FET CHARACTERISTICS & SCR

PRESENTED BY

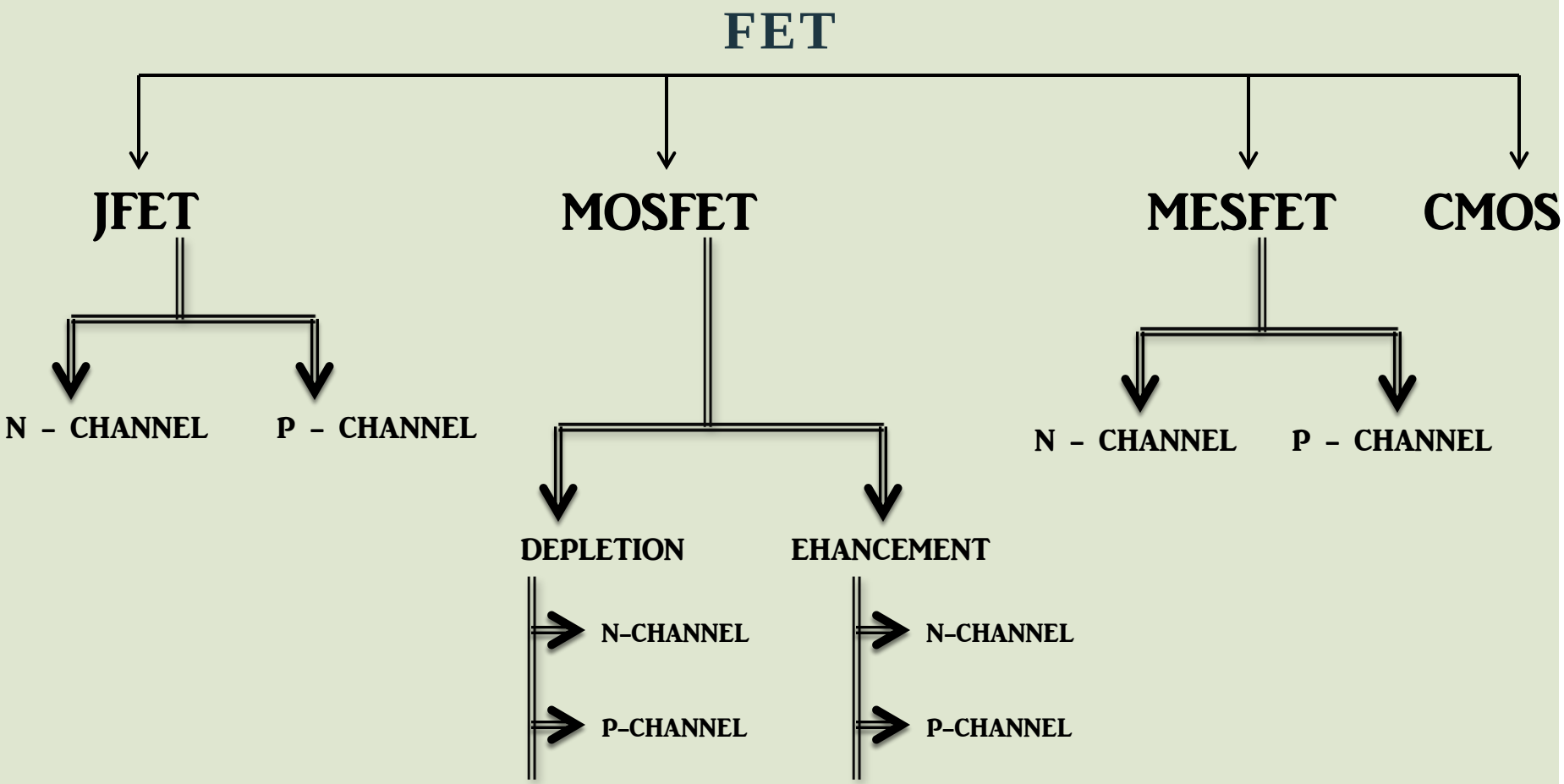
GOUTHAM V

ASST. PROF. DEPT. OF ECE
BGSIT, B G NAGARA

Introduction to FET:

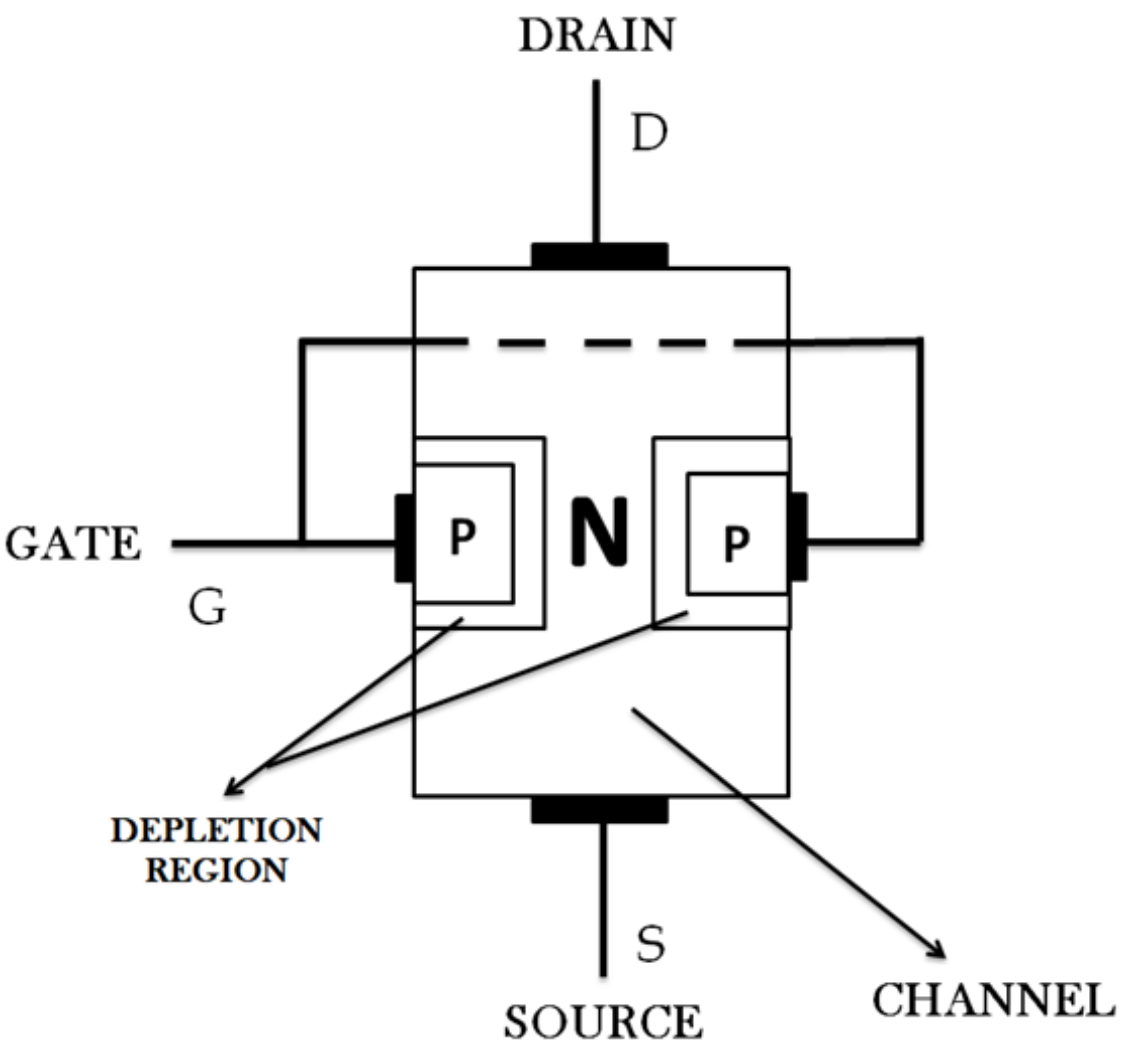
- FET is the abbreviation of **Filed Effect Transistor**.
- FET's are **unipolar** devices.
- FET's are semiconductor device, which has three terminals named as Source(S), Drain(D) and Gate(G), which are used as Amplifiers or Switches.
- Gate terminal acts as controlling terminal, i.e. the voltage applied between the gate and the source terminal control the output drain current I_D. Hence FET's are called as **Voltage Controlled Devices.**
- FET's are categorised as:
  - ***Junction Field Effect Transistors [JFET].***
  - ***Metal Oxide Semiconductor Field Effect Transistor [MOSFET].***
  - ***Metal Semiconductor Field Effect Transistors [MESFET].***

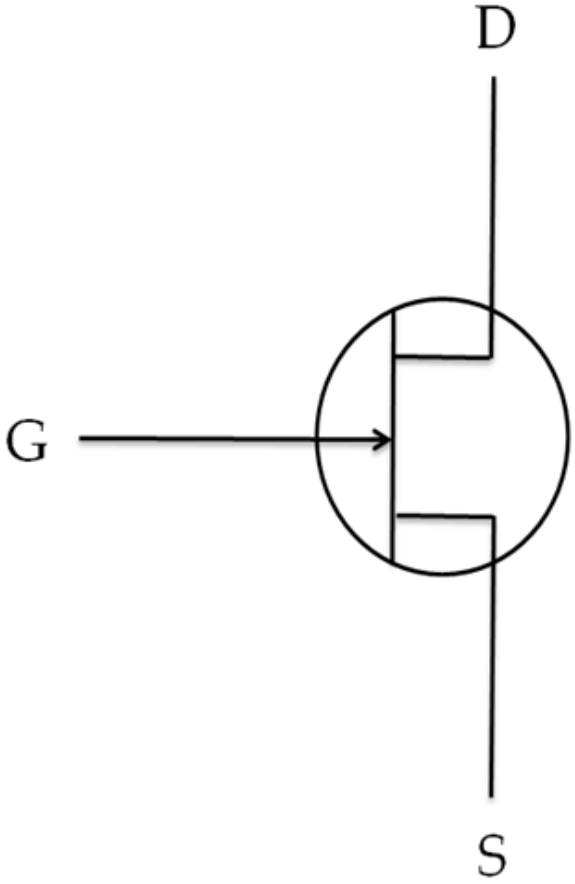
CLASSIFICATION OF FET



JUNCTION FIELD EFFECT TRANSISTOR:

N – CHANNEL JFET





SYMBOLIC REPRESENTATION

JUNCTION FIELD EFFECT TRANSISTOR:

N – CHANNEL JFET

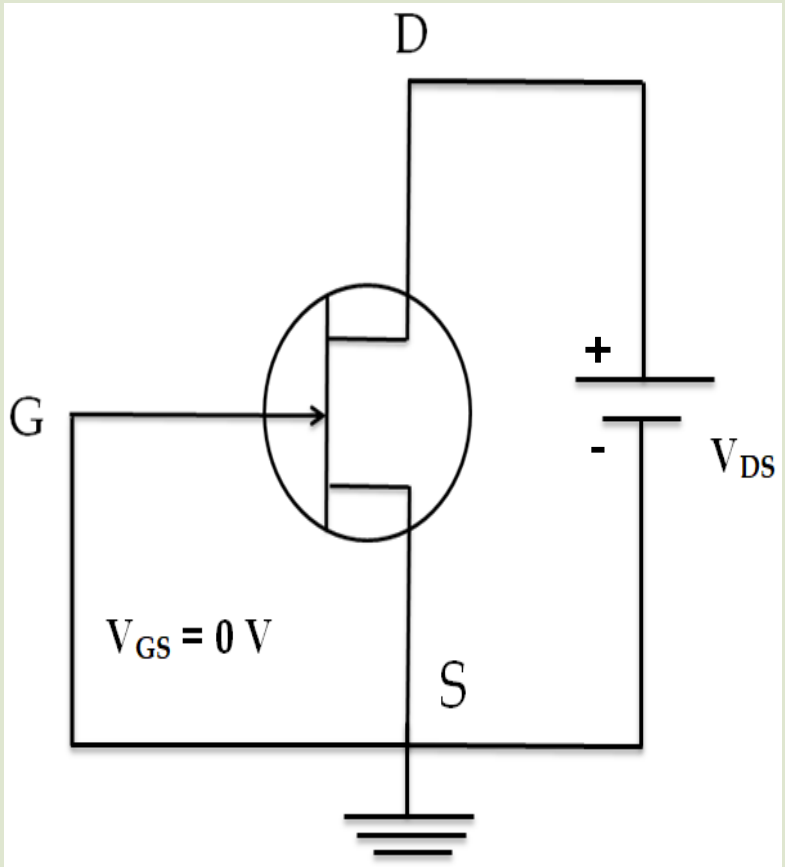
Construction:

- In an n-channel JFET, an N-type semiconductor material forms a channel between embedded layers of P-type material.
- Hence two P-N junctions are formed between the semiconductor channel and the embedded semiconductor layers.
- Ohmic contacts or Metal contacts are placed at the top and bottom of the channel and are referred to as the **Drain (D)** and the **Source(S)** terminals.
- The channel behaves as an resistive element between drain and source terminal.
- In an N-channel JFET, both the embedded P-type layers are connected together and form the GATE(G) terminal.

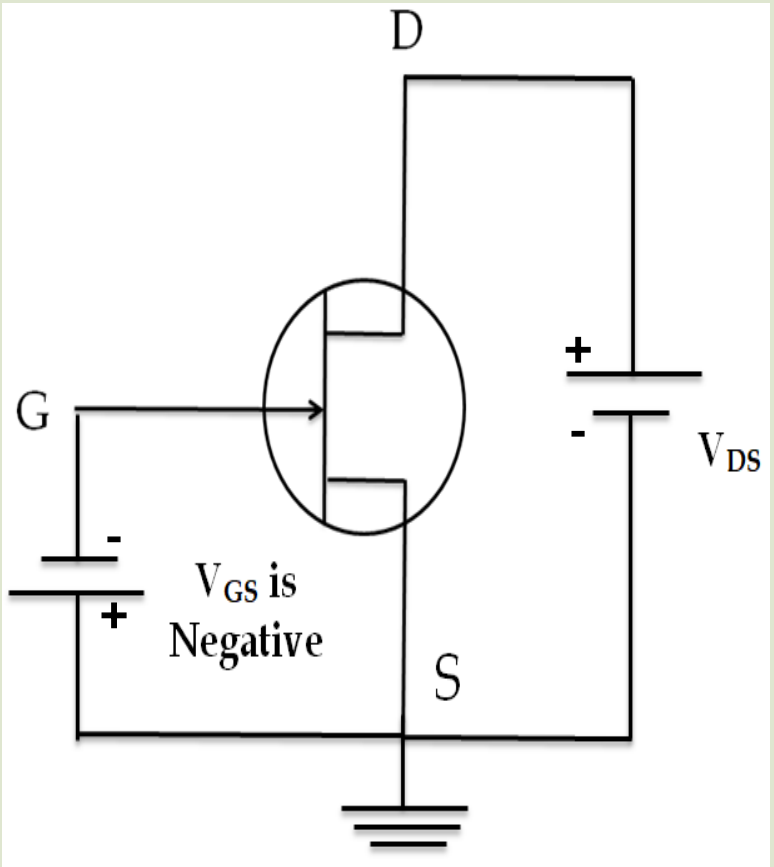
OPERATION

- We study the Operation of N-channel JFET in Two conditions:

1. V_{GS} is 0 V



2. V_{GS} is NEGATIVE



JUNCTION FIELD EFFECT TRANSISTOR:

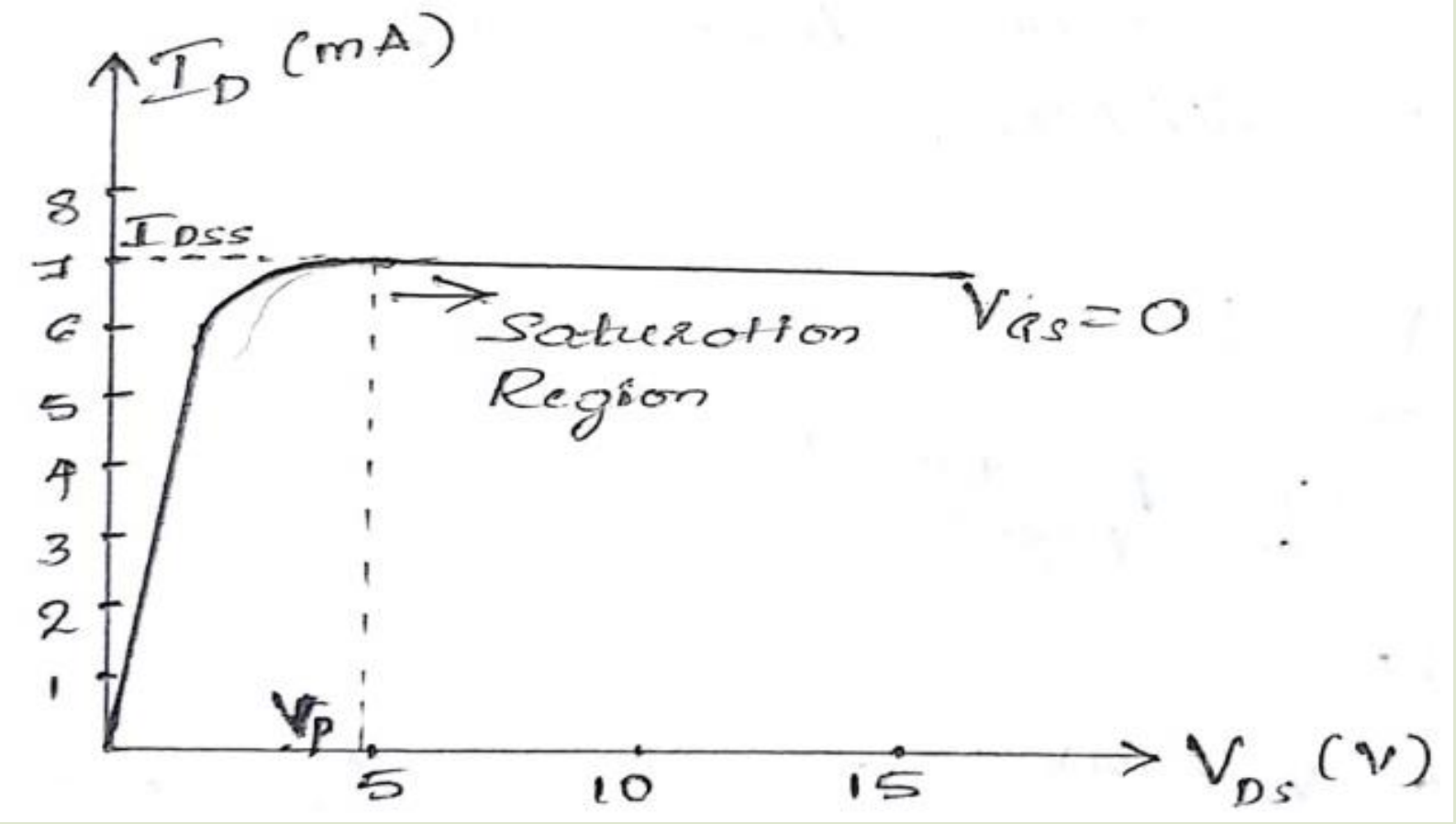
N – CHANNEL JFET

Operation and Characteristics:

- Let us consider N-channel JFET, to which a ***positive drain-source voltage*** **(V_{DS})** is applied with gate terminal shorted to the source terminal **($V_{GS} = 0$)**.
- When the positive drain source voltage is applied, the ***electrons in the N-channel are attracted to the drain terminal establishing flow of drain current I_D,*** whose value is determined by the value of the applied V_{DS} and the resistance of the N-channel between the drain and the source terminal.
- Due to the flow of I_D, there will be uniform voltage drop above the channel resistance which reverse bias the Two PN junction which results in increasing the width of the depletion region.
- ***I_D increases with increase in the V_{DS}*** till the V_{DS} reach a point of saturation. ***The value of the V_{DS} where the I_D gets saturated*** is referred to as the ***Pinch-Off voltage (V_P)***.

- When V_{DS} ***reaches*** V_P, the value of I_D doesn't changes with further increase in the value of V_{DS} which is called as ***Pinch off condition***.
- Therefore I_D essentially remains constant for $V_{DS} > V_P$.

- This current is called as ***Drain to Source current for short circuit connection between gate and source [I_{DSS}]***.



When V_{GS} is Applied:

- In n-channel JFET, the voltage V_{GS} is negative, that's the gate terminal is made more negative than the source terminal.

- When a negative voltage is applied to the gate terminal, there is increase in the width of depletion region. As the value of $\mathbf{V_{GS}}$ becomes more negative, the value of saturation current decreases further and drain current becomes zero for $\mathbf{V_{GS}}$ equal to $\mathbf{-V_P}$.
- The left region of the locus of the pinch-off voltage is the Ohmic region or the voltage controlled region. In Ohmic region, JFET acts as a variable resistor, whose resistance is controlled by the applied gate-source voltage.
- Region to the right of the locus of the pinch-off voltage is the saturation region.
- Drain resistance in the saturation region is given by;

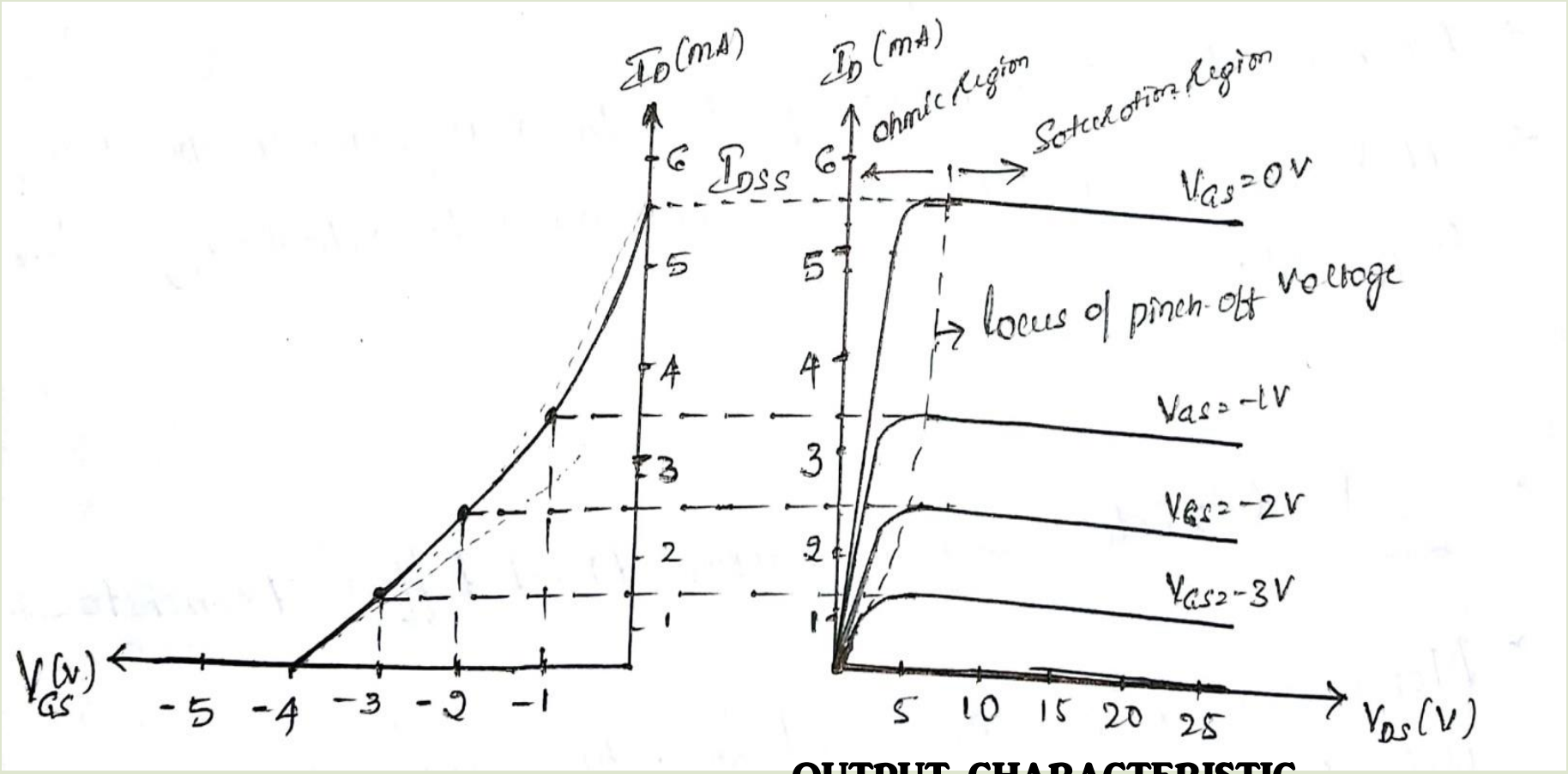
$$r_d = \frac{r_o}{(1 - \frac{V_{GS}}{V_P})^2}$$

- Relationship between the output current ID in the saturation region for the given value of input voltage VGS is given by the below equation which is called as Shockley's equation;

$$\mathbf{I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2}$$

- Drain characteristics of the JFET is plotted between $\mathbf{I_D}$ and $\mathbf{V_{DS}}$ for $\mathbf{V_{GS} = 0\ V}$.
- Transfer characteristics are plotted between $\mathbf{I_D}$ and $\mathbf{V_{GS}}$, which can also be plotted using Shockley's equation.
- Characteristic curve is plotted between $\mathbf{I_D}$ and $\mathbf{V_{DS}}$ for different values of $\mathbf{V_{GS}}$.

The transfer characteristic curve and the output/total characteristic curve is as shown below.



TRANSFER CHARACTERISTIC CURVE

OUTPUT CHARACTERISTIC CURVE

JFET- Construction and Working Explained.mp4

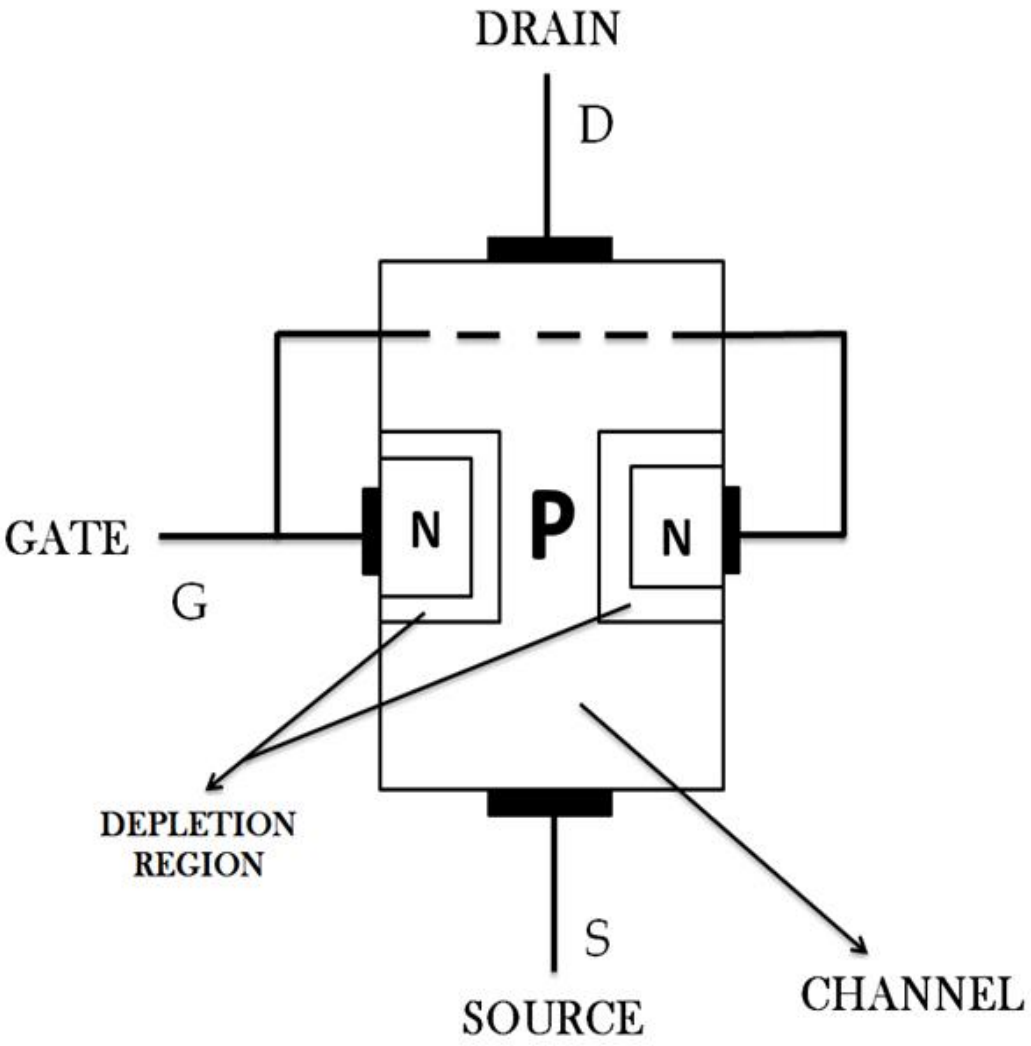
JUNCTION FIELD EFFECT TRANSISTOR:

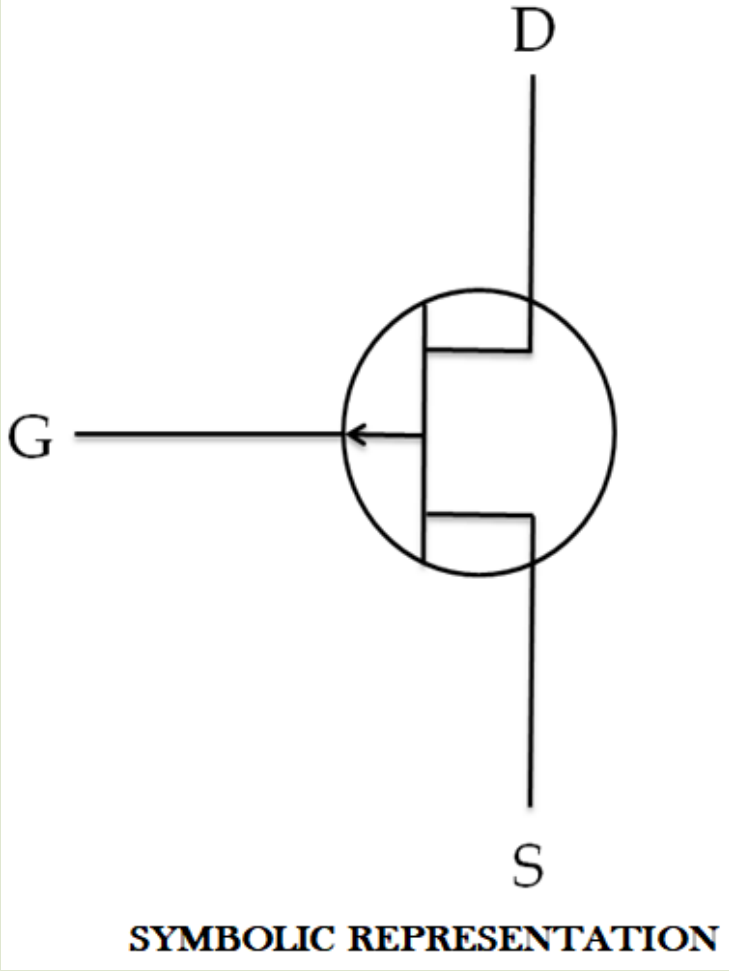
P – CHANNEL JFET

Construction:

- In an p-channel JFET, an p-type semiconductor material forms a channel between embedded layers of n-type material.
- Hence two P-N junctions are formed between the semiconductor channel and the embedded semiconductor layers.
- Ohmic contacts or Metal contacts are placed at the top and bottom of the channel and are referred to as the Drain(D) and the Source(S) terminals.
- The channel behaves as a resistive element between drain and source terminal.
- In an P-channel JFET, both the embedded N-type layers are connected together and form the GATE(G) terminal.

Figure below shows the cross section of p-channel JFET with its symbolic representation.



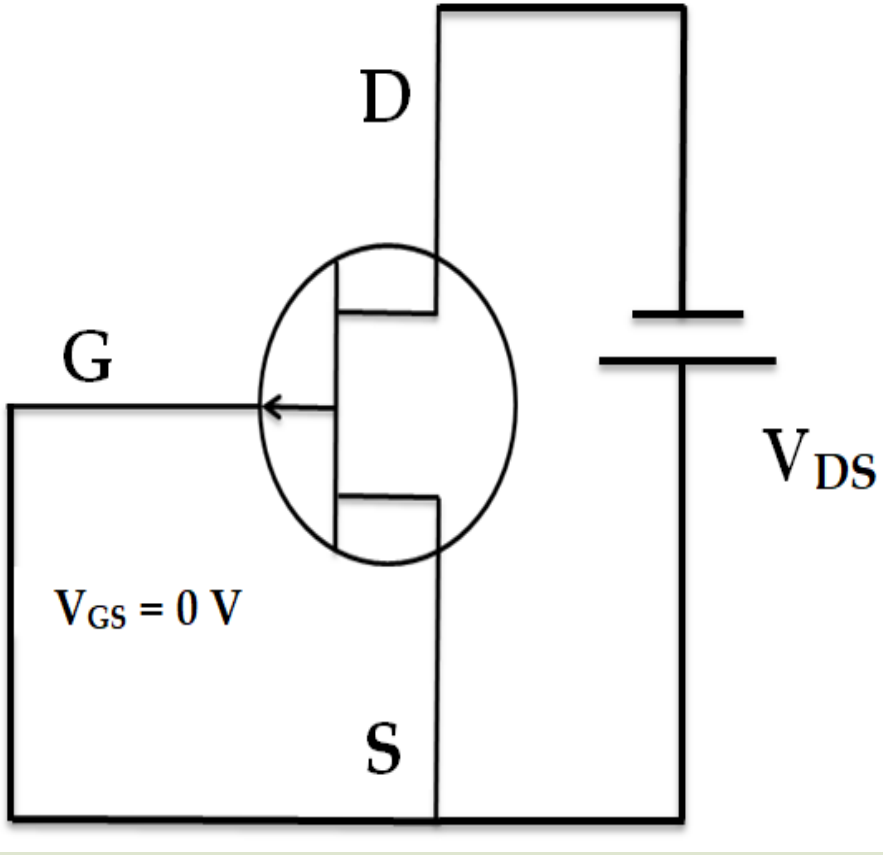


SYMBOLIC REPRESENTATION

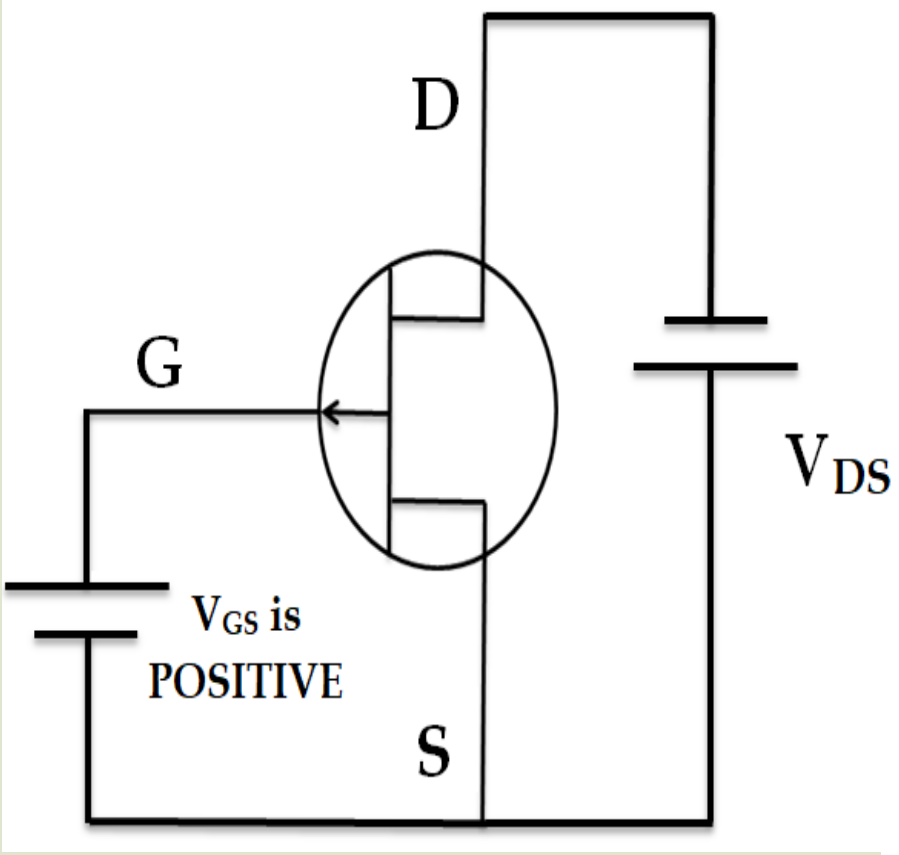
OPERATION

- We study the Operation of P-channel JFET in Two conditions:

1. V_{GS} is 0 V



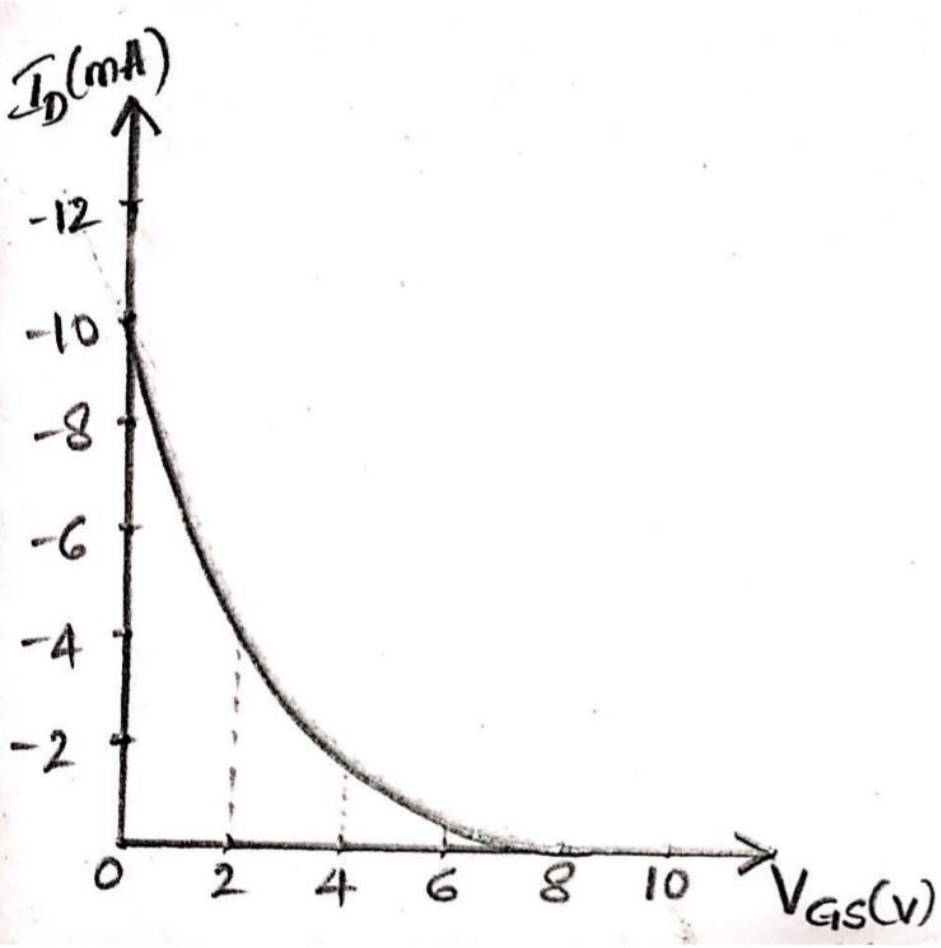
2. V_{GS} is POSITIVE



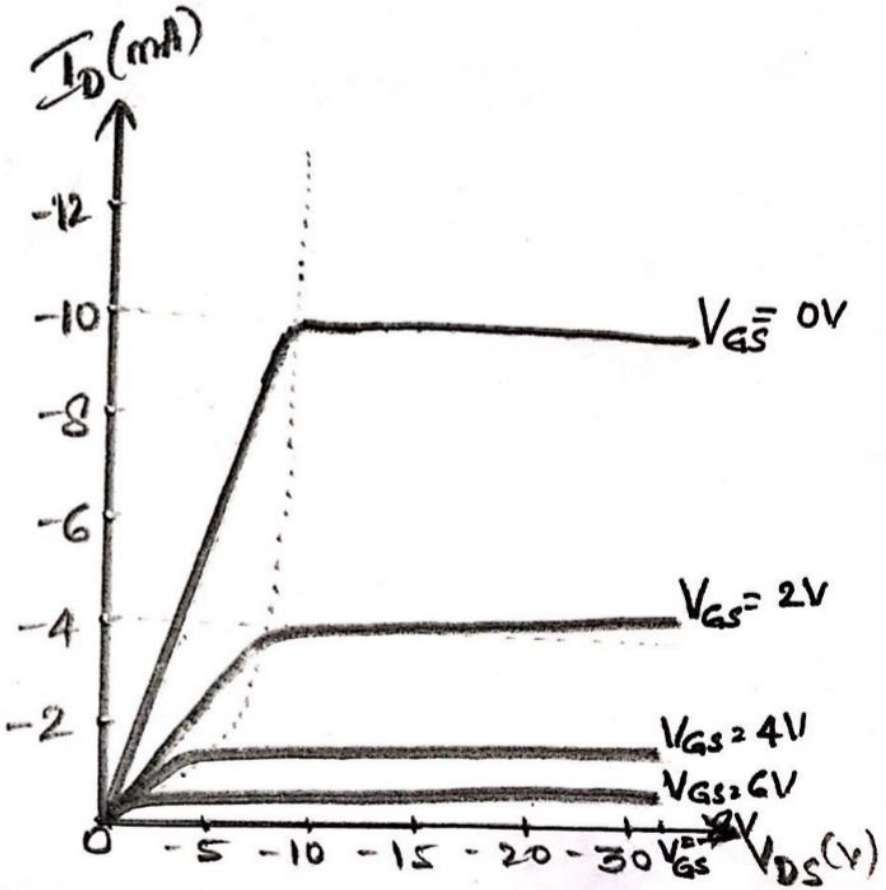
OPERATION:

- A voltage source is connected between Drain and Source terminals ($\mathbf{V_{DS}}$) making drain negative and source positive. Gate and Source terminals are shorted ($\mathbf{V_{GS} = 0}$).
- The region between the two doped n-substrate acts as channel.
- Electrons attracts holes inducing **Negative Drain Current** ($\mathbf{I_D}$) which gets increases linearly with the increase of $\mathbf{V_{DS}}$ and gets saturated for further increasing of $\mathbf{V_{DS}}$.
- A voltage source is connected between Gate and Source terminal **($\mathbf{V_{GS}}$)** making gate positive and source negative.
- By applying positive gate to source voltage **($\mathbf{V_{GS}}$)**, it controls the flow of $\mathbf{I_D}$ as shown in the characteristic curve.
- At $\mathbf{V_{GS} = - V_P}$, $\mathbf{I_D}$ becomes zero.

- The characteristic curve is shown below.



TRANSFER CHARACTERISTIC CURVE



OUTPUT CHARACTERISTIC CURVE

METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR [MOSFET]

- Metal Oxide FET is insulated from the semiconductor channel by a very thin oxide layer.
- MOSFET's are classified into two types, depending on their construction and mode of operation:
  - ***Depletion Type MOSFET*** ***[DE-MOSFET]***
  - ***Enhancement Type MOSFET*** ***[E - MOSFET]***

Depletion MOSFET:

"The device which conducts under zero gate bias are called or zero gate voltage are called Depletion MOSFET".

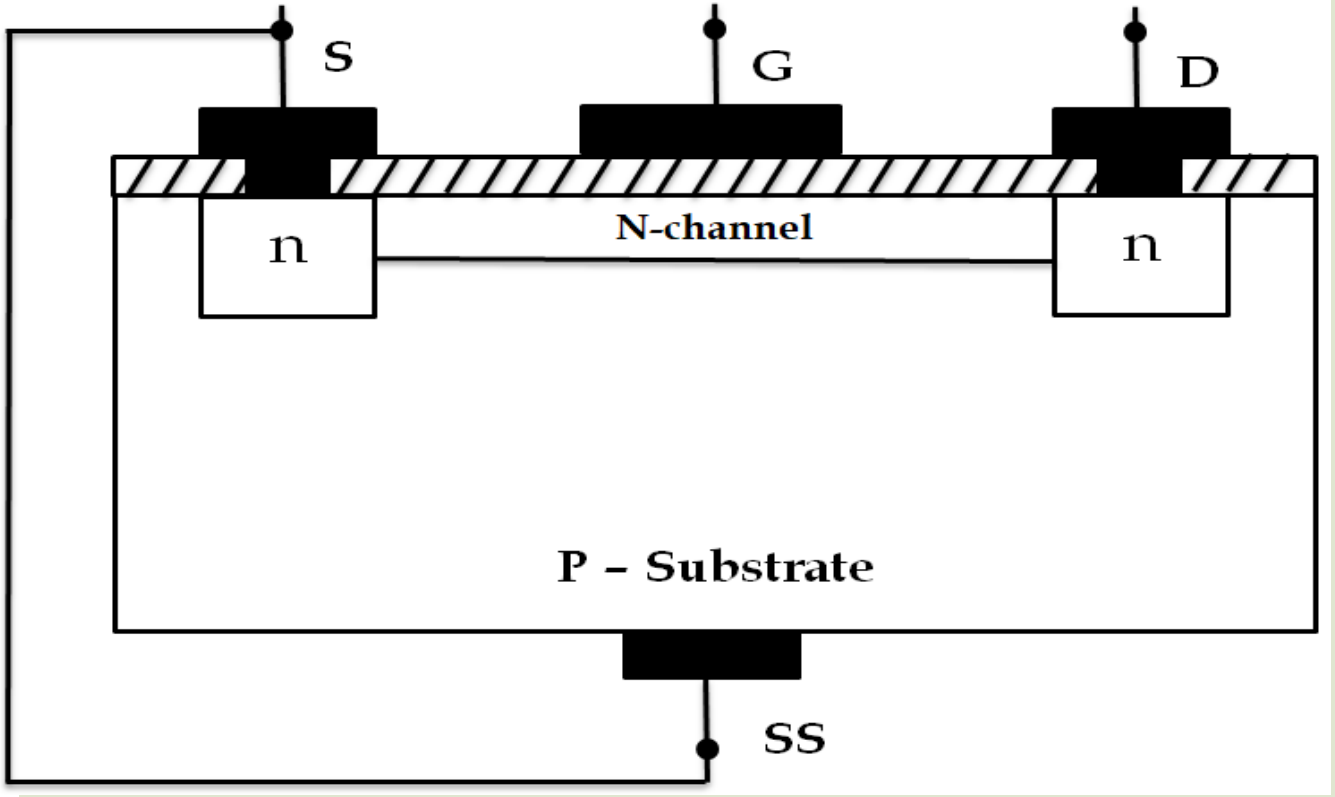
In this type, there is a physical channel present between Source and Drain terminal.

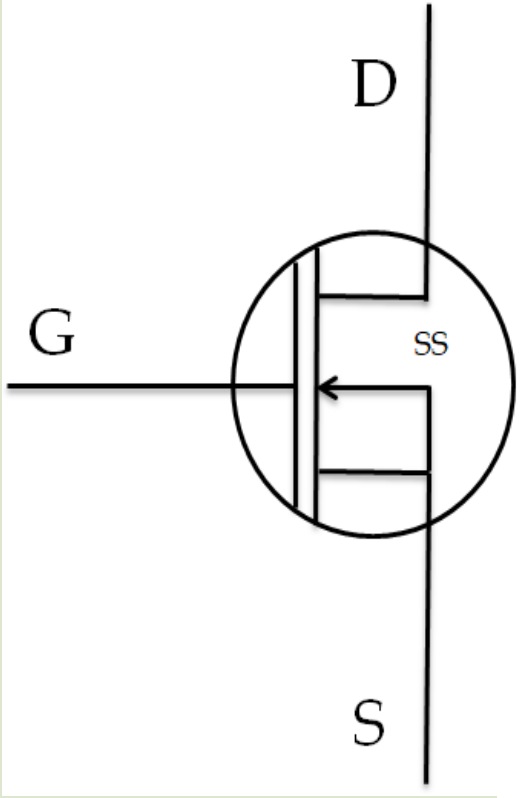
Enhancement MOSFET:

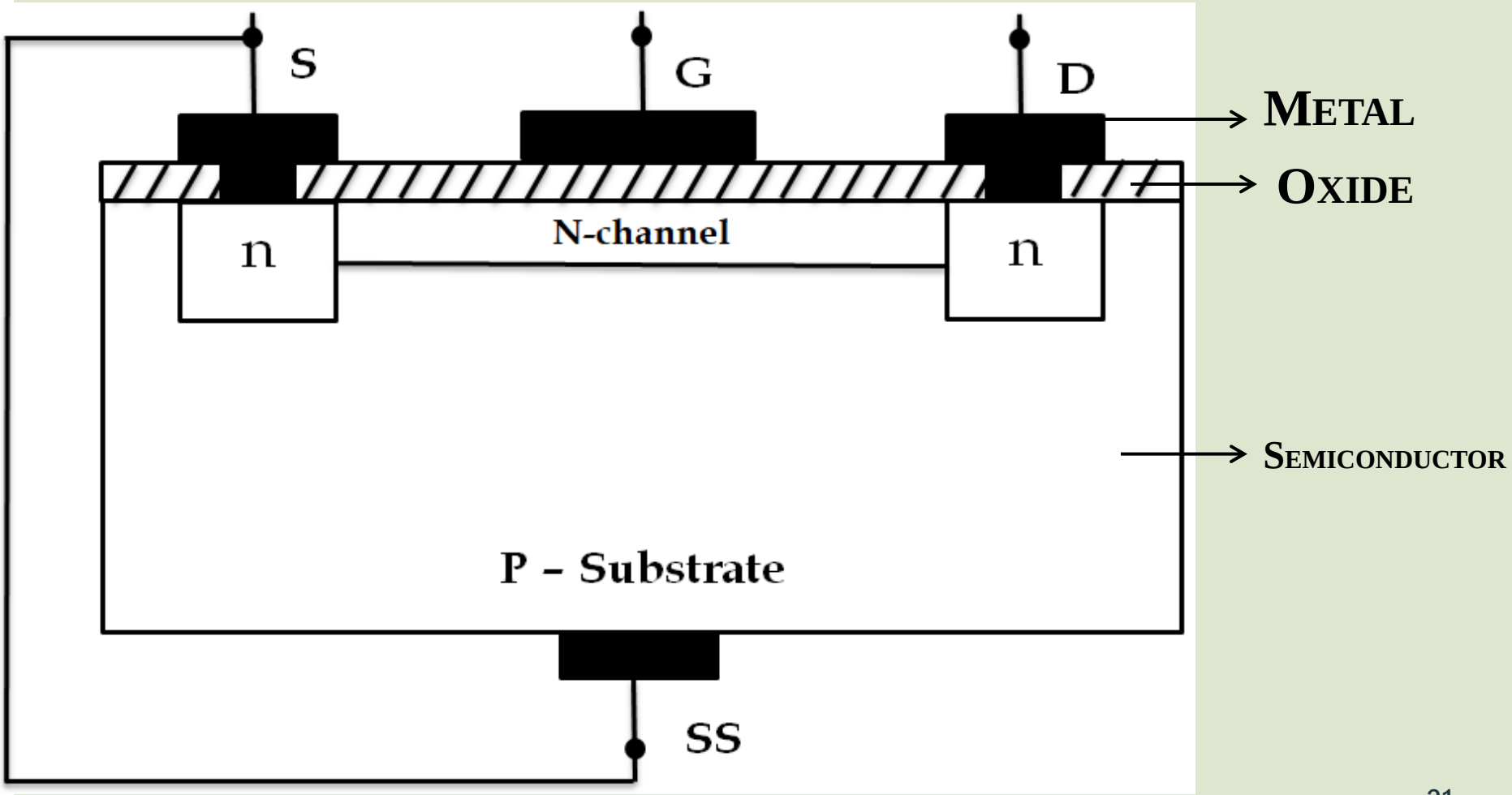
"The device which do not conducts under zero gate bias are called or zero gate voltage are called Enhancement MOSFET".

In this type, there is no physical channel between Source and Drain terminal.

N-CHANNEL DEPLETION TYPE MOSFET:



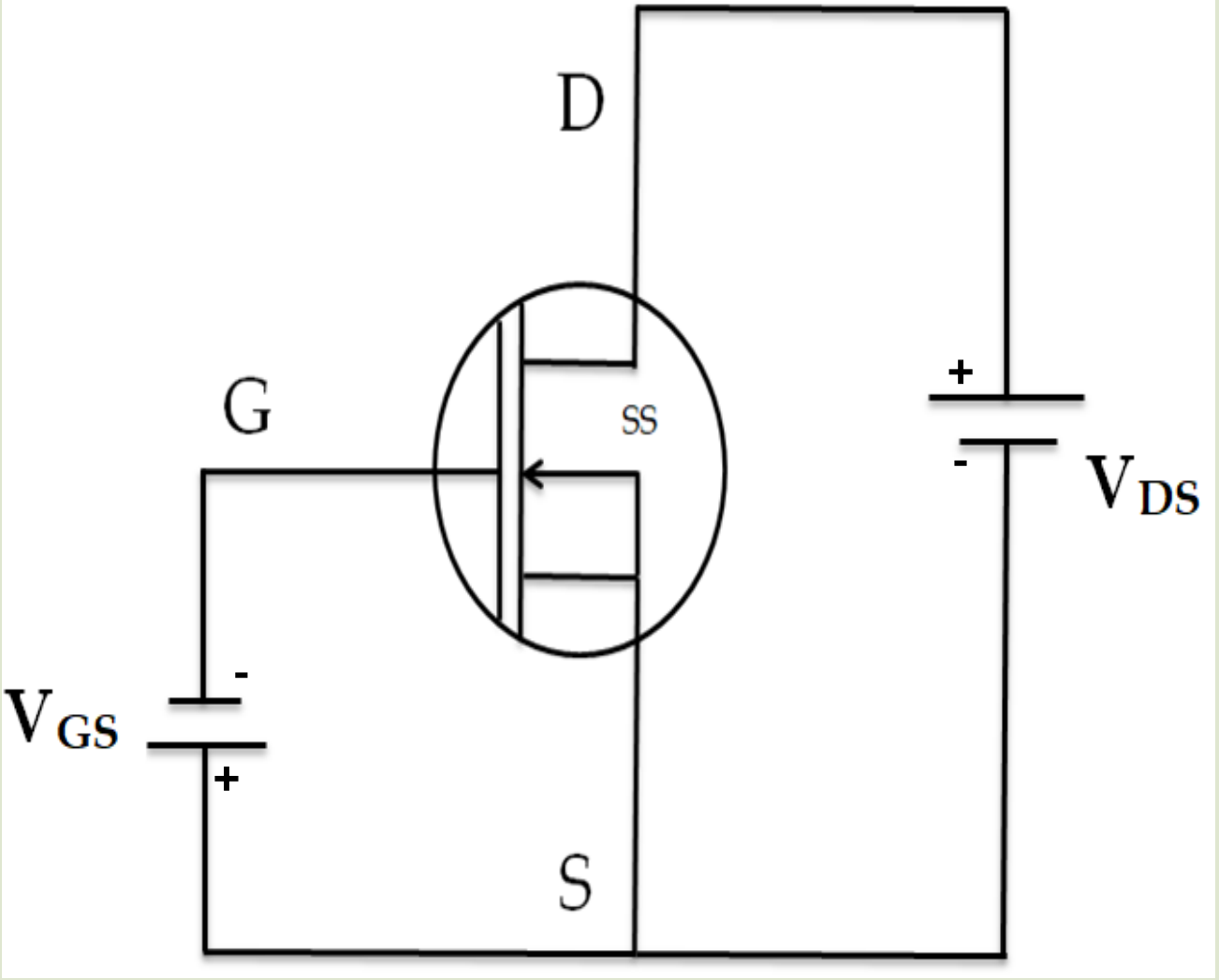



S
G
D
METAL
OXIDE
n
N-channel
n
SEMICONDUCTOR
P – Substrate
SS

CONSTRUCTION:

- Consider a slab of P-type substrate which is attached with a metallic contact called as Substrate terminal(SS).
- Two N-type materials are doped in the p-type substrate which is connected through the metallic contacts, which forms the two terminals namely Source(S) and Drain(D).
- Between these two N-type regions, an N channel is formed on the P-type substrate which acts as a gate terminal. But a very thin silicon oxide[SiO_2] layer separates the metal of the gate terminal from the channel.
- The N-channel Depletion type MOSFET is as shown below with its symbolic representation.

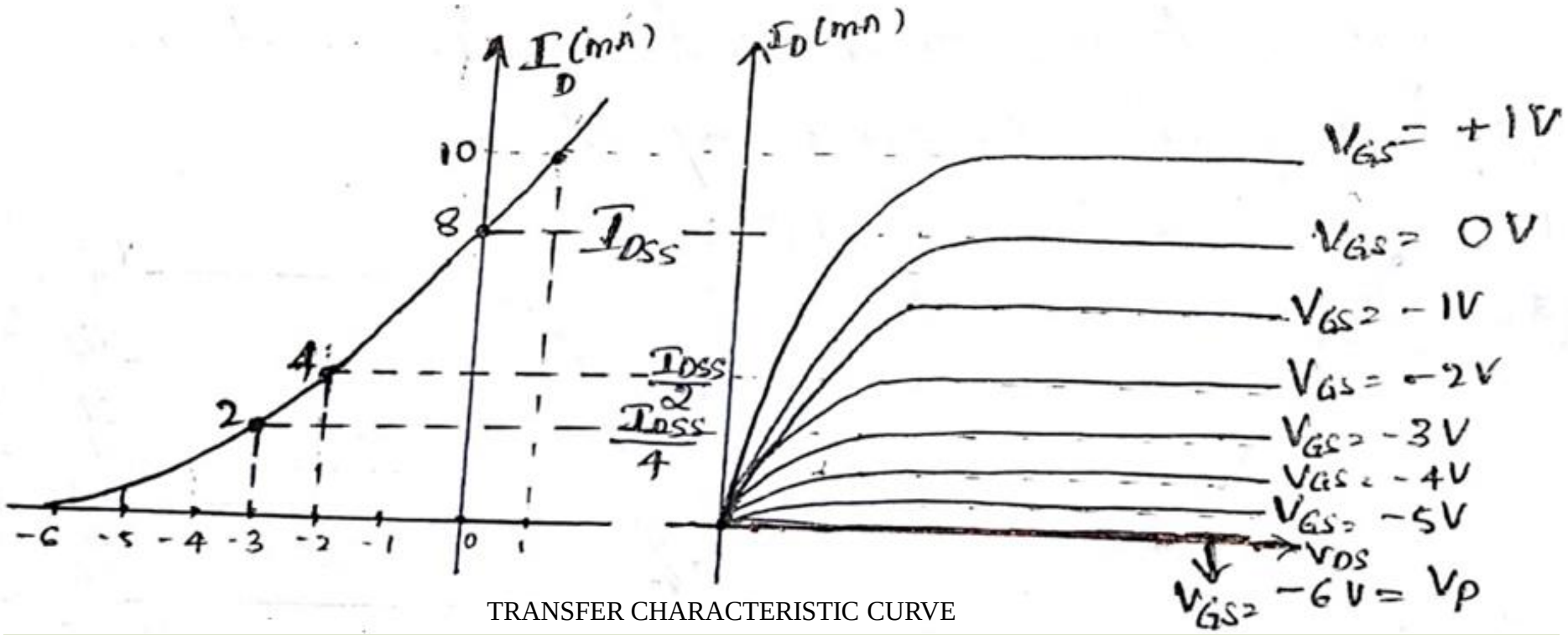
OPERATION:



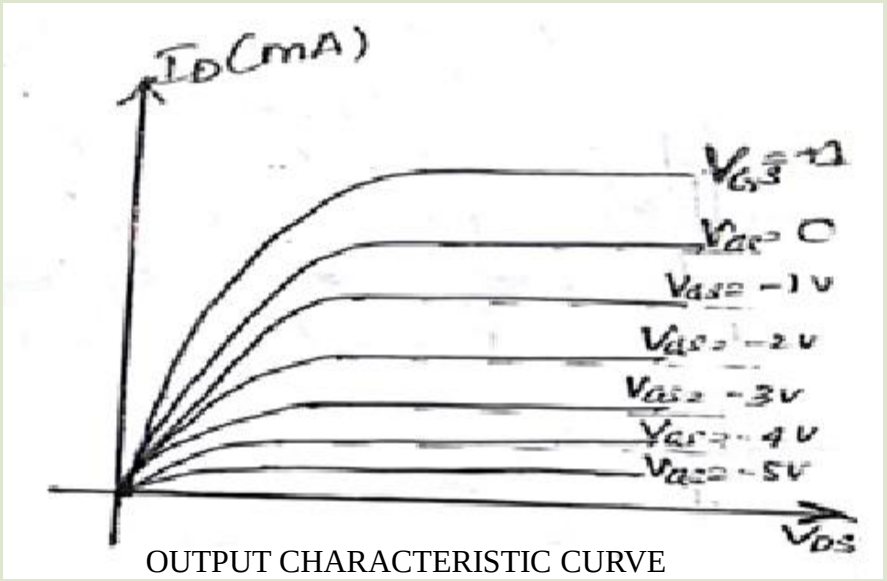
OPERATION:

- First the gate to source voltage is set 0 volts ($\mathbf{V_{GS} = 0}$) by the direct connection from one terminal to other. [i.e. shorted].
- Voltage $\mathbf{V_{DS}}$ is applied across the drain to source terminal which makes drain more positive than source.
- By making drain more positive, the positive potential at the drain attracts the electrons from the source through the n channel which induces the **Drain Current $\mathbf{I_D}$**.
- The resulting current at $\mathbf{V_{GS} = 0V}$ is labelled as $\mathbf{I_{DSS}}$.
- When the gate terminal is at negative potential as compared to the source terminal, electrons in the N-channel are repelled by this negative potential towards the P-type substrate and also the holes in the P-type substrate are attracted towards the gate and recombination takes place results in reduction of free electrons in the N-channel.

- When the gate terminal is at negative potential as compared to the source terminal, electrons in the N-channel are repelled by this negative potential towards the P-type substrate and also the holes in the P-type substrate are attracted towards the gate and recombination takes place results in reduction of free electrons in the N-channel.
- Higher the negative potential, more is the recombination and less the number of free electrons in the channel. Hence the drain current decreases with increase in the value of negative gate-source potential.
- The region for zero and negative value of gate-source voltage is referred to as the Depletion region.
- Figure below shows the N-channel DE MOSFET transfer characteristics and output characteristics.

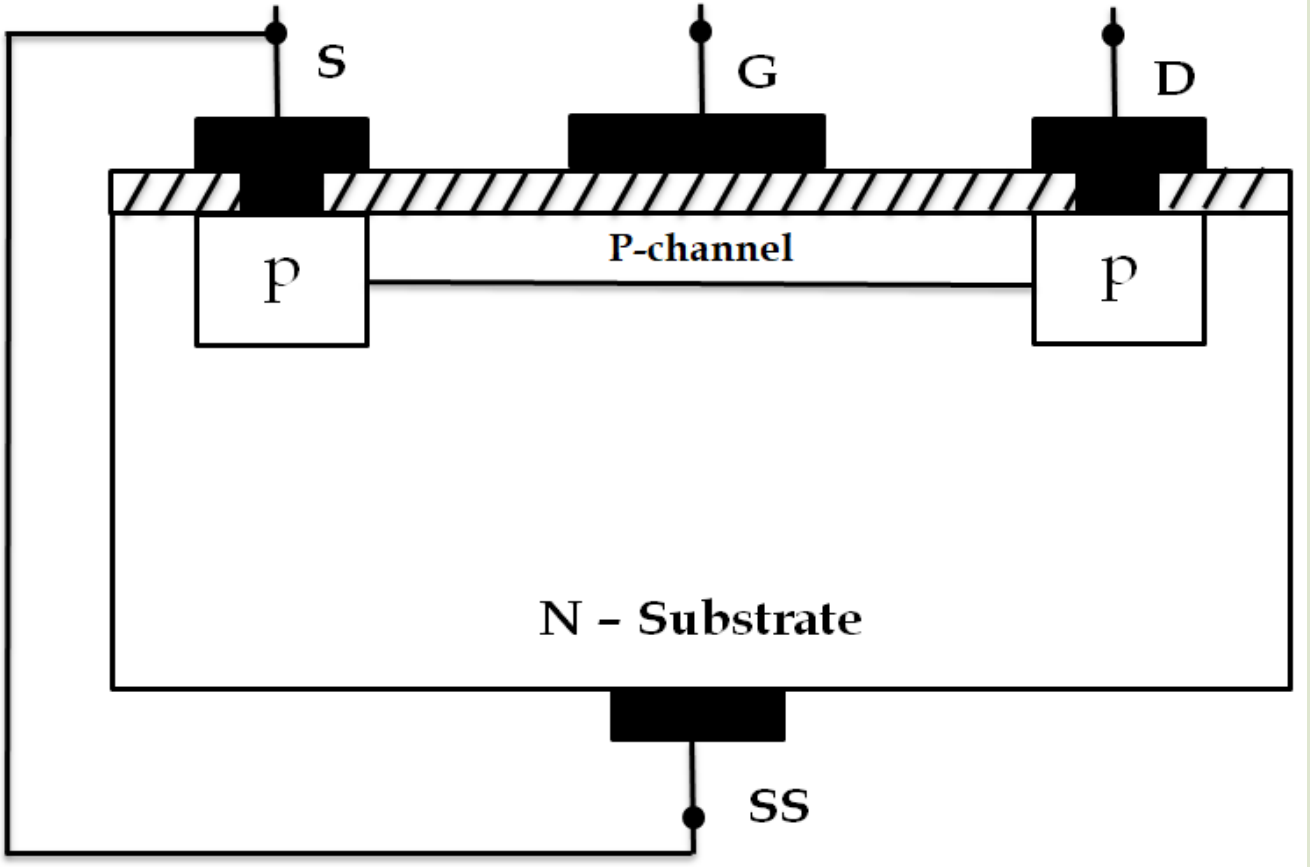


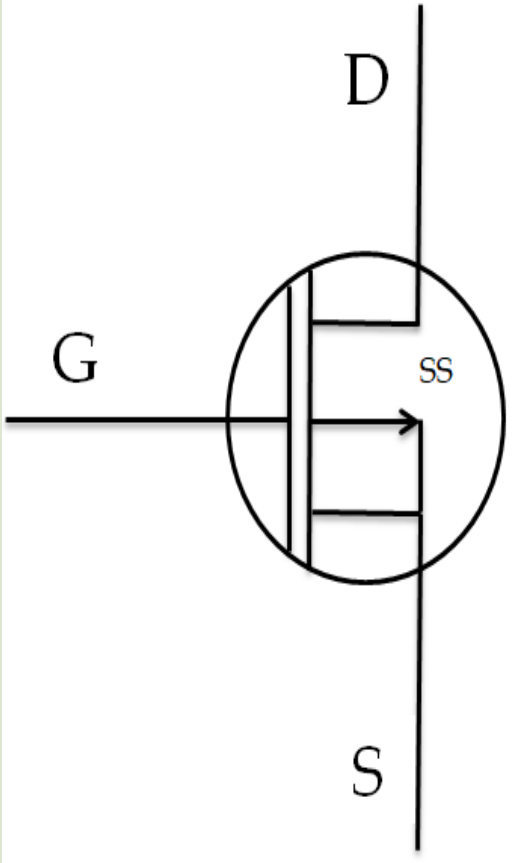
TRANSFER CHARACTERISTIC CURVE



OUTPUT CHARACTERISTIC CURVE

P-CHANNEL DEPLETION TYPE MOSFET:

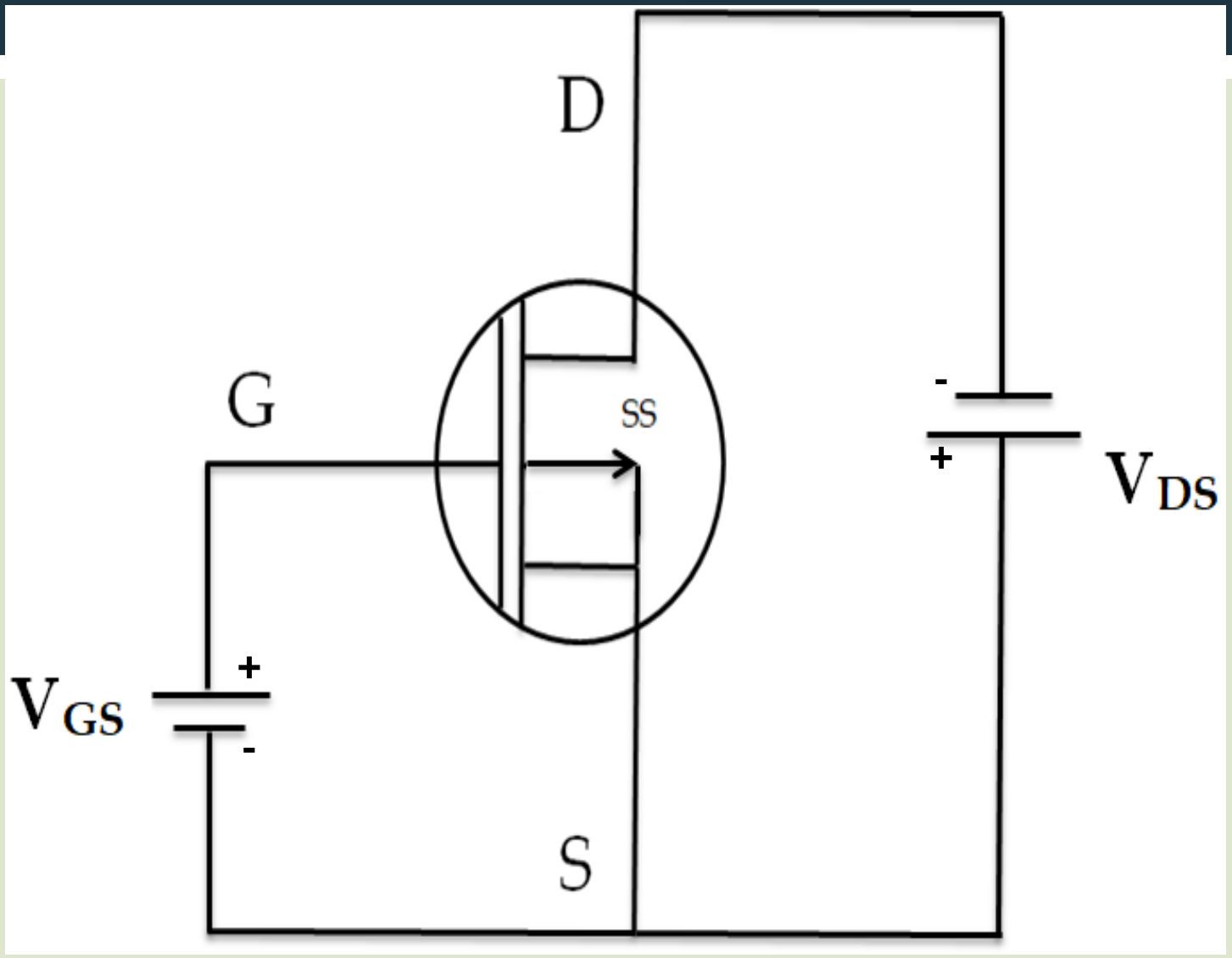




CONSTRUCTION

- Consider a slab of P-type substrate which is attached with a metallic contact called as Substrate terminal (SS).
- Two N-type materials are doped in the p-type substrate which is connected through the metallic contacts, which forms the two terminals namely Source(S) and Drain(D).
- Between these two N-type regions, an N channel is formed in the P-type substrate which acts as a gate terminal. But a very thin silicon oxide **[SiO_2]** layer separates the metal of the gate terminal from the channel.
- The N-channel Depletion type MOSFET is as shown with its symbolic representation.

OPERATION



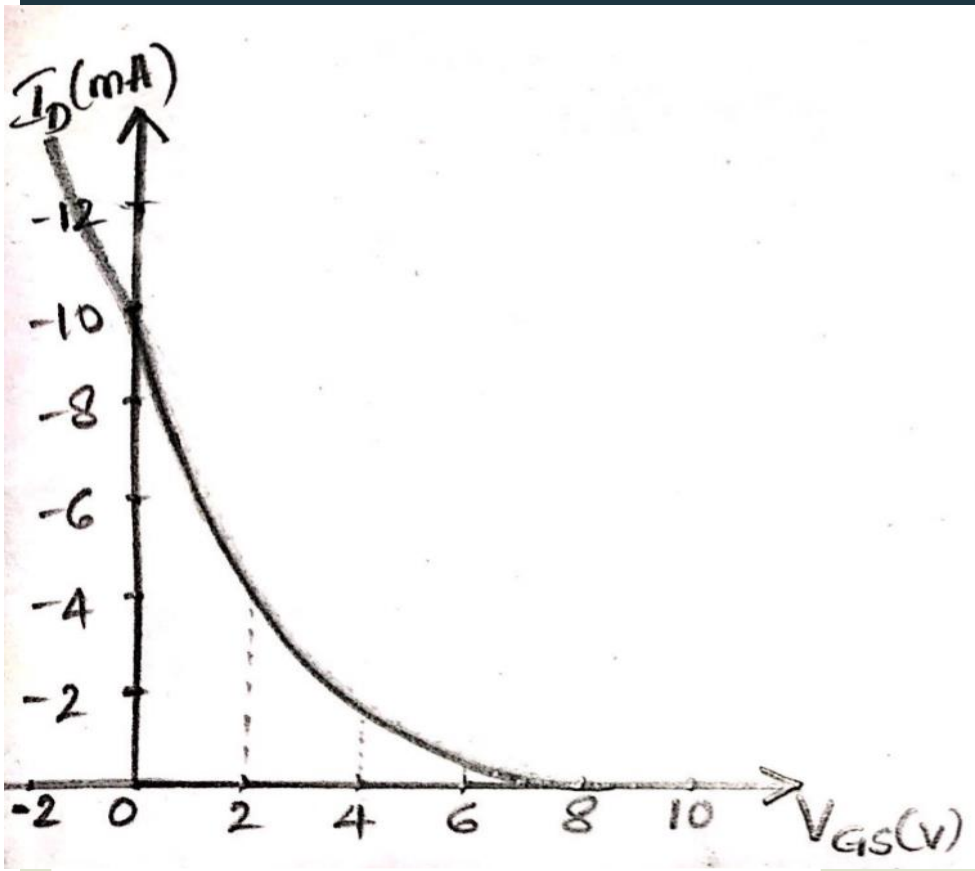
OPERATION

- The gate to source voltage is set 0 volts ($\mathbf{V_{GS} = 0}$) by the direct connection from one terminal to other. [i.e. shorted].
- A voltage source is connected between drain and source terminal making drain negative and source positive ($\mathbf{V_{DS}}$).
- By making drain more negative, the negative potential at the drain attracts the holes from the source through the p-channel which induces the **Negative Drain Current $\mathbf{I_D}$**. The resulting current at $\mathbf{V_{GS} = 0V}$ is labelled as $\mathbf{I_{DSS}}$.
- When the gate terminal is at positive potential as compared to the source terminal, **holes** in the P-channel are repelled by this positive potential towards the N-type substrate and also the electrons in the N-type substrate are attracted towards the gate and recombination takes place results in reduction of free holes in the P-channel.

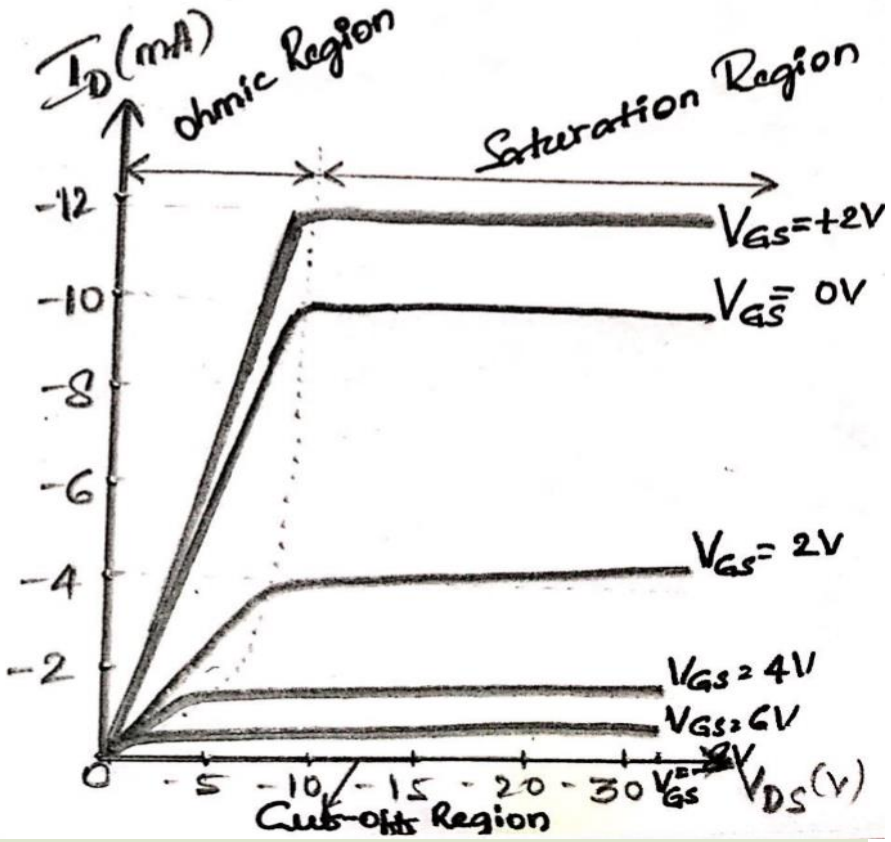
- Higher the positive potential, more is the recombination and less the number of free holes in the channel. Hence the drain current decreases with increase in the value of positive gate-source potential.

- The region for zero and positive value of gate-source voltage is referred to as the Depletion region.

- Figure below shows the circuit connection of biasing of P-channel DE MOSFET and the transfer characteristics and output characteristics.



TRANSFER CHARACTERISTIC CURVE



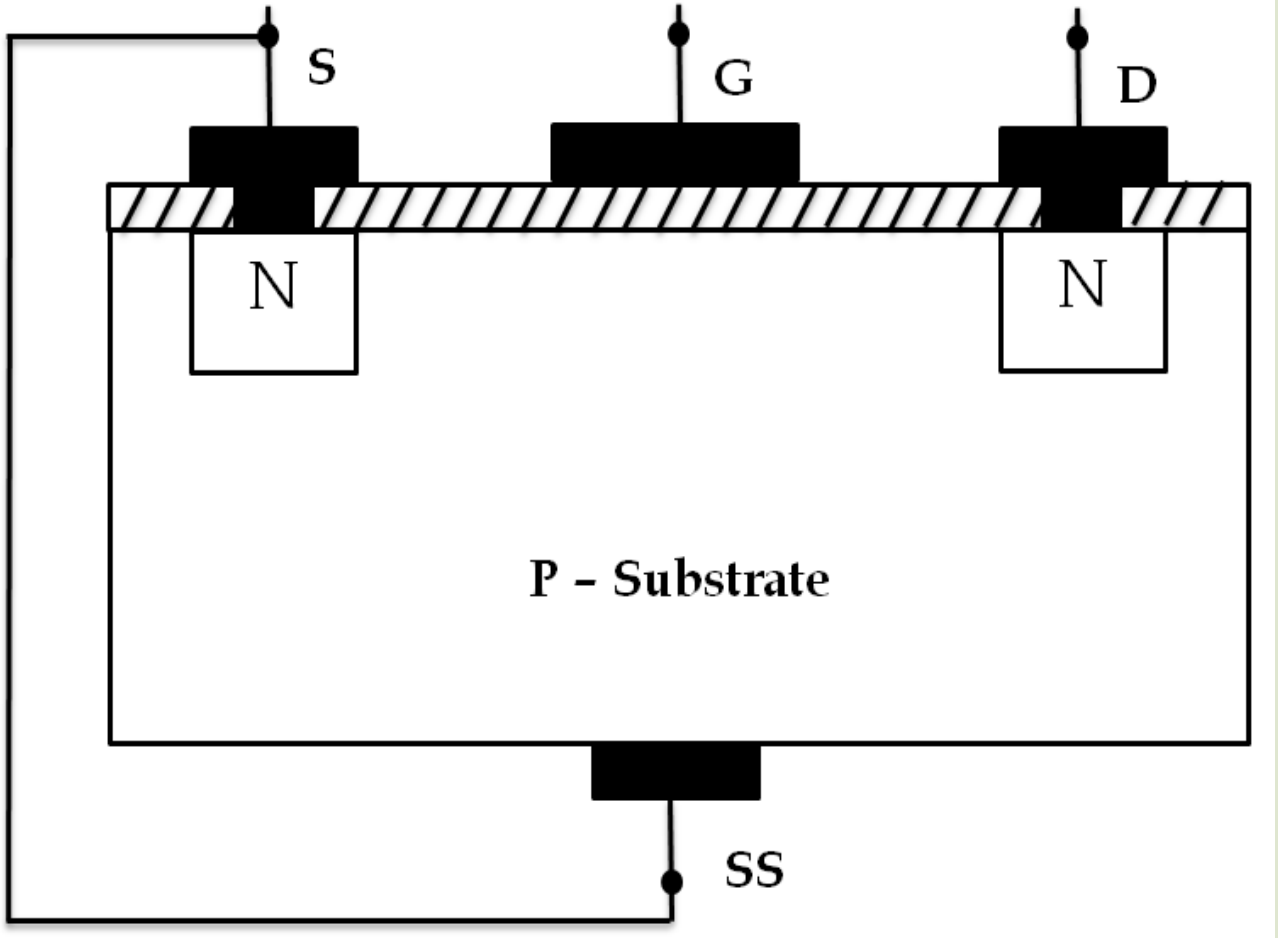
TOTAL/OUTPUT CHARACTERISTIC CURVE

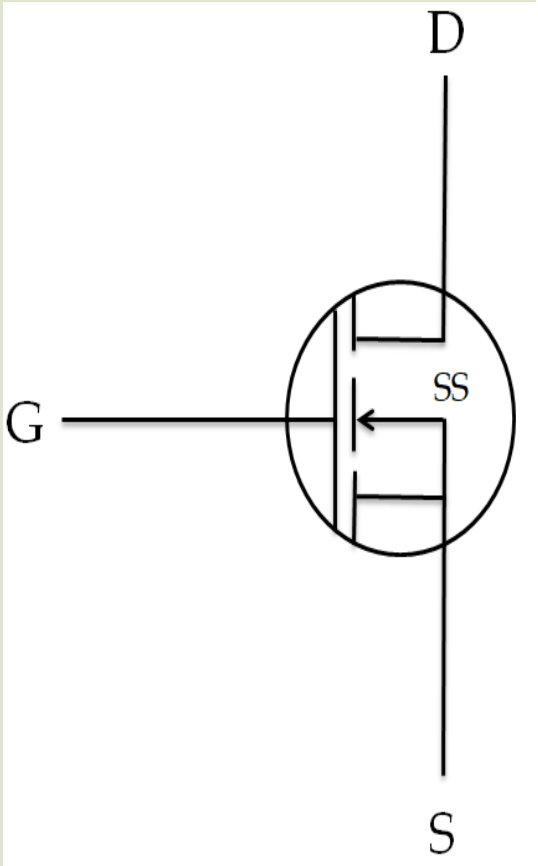
ENHANCEMENT MOSFET:

Enhancement MOSFET:

- Here the physical channel is not present.
- Drain current will be cut-off until the gate-to-source **[V_{GS}]** voltage reaches a specific magnitude.

N-CHANNEL E-MOSFET:



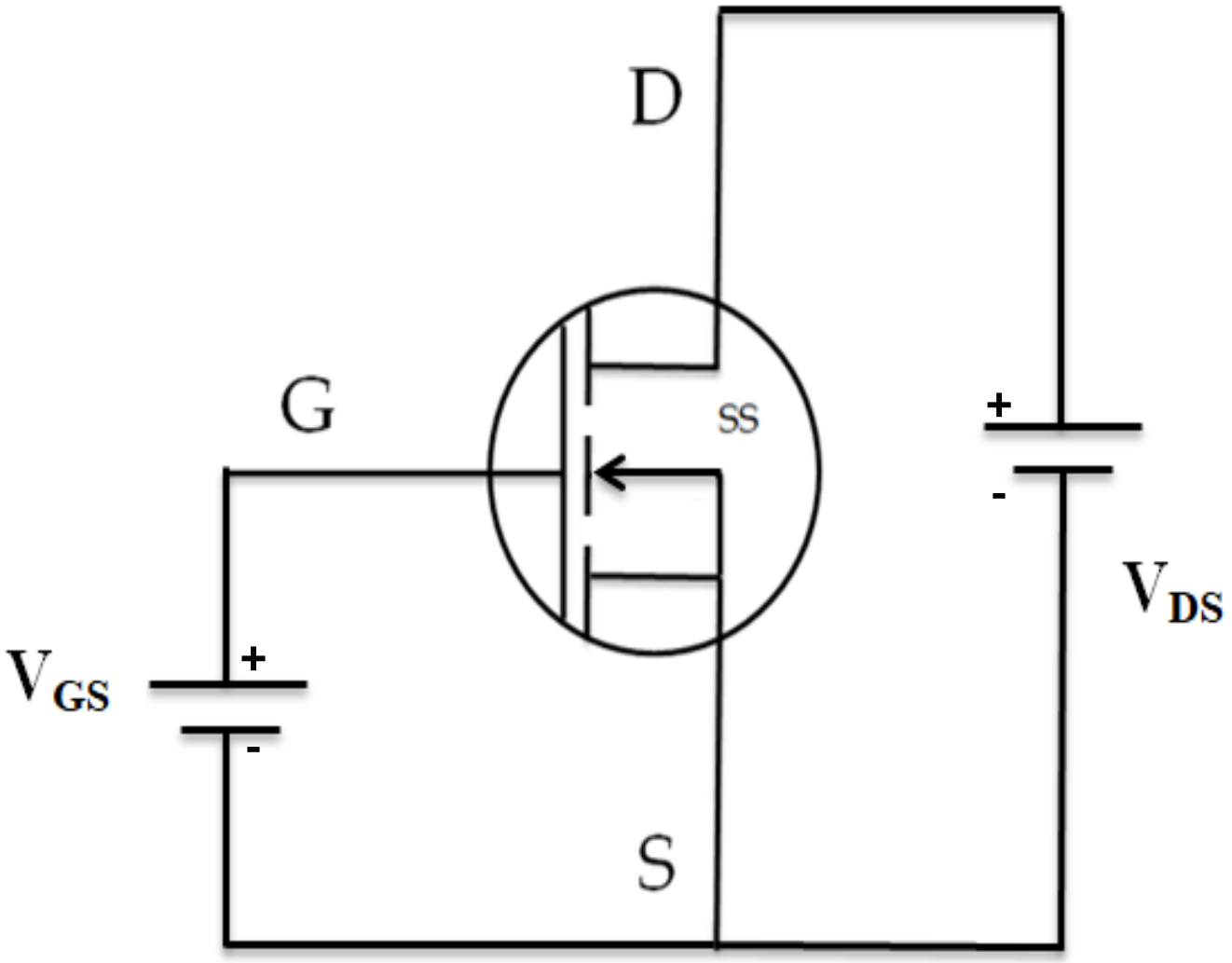


N-CHANNEL E-MOSFET:

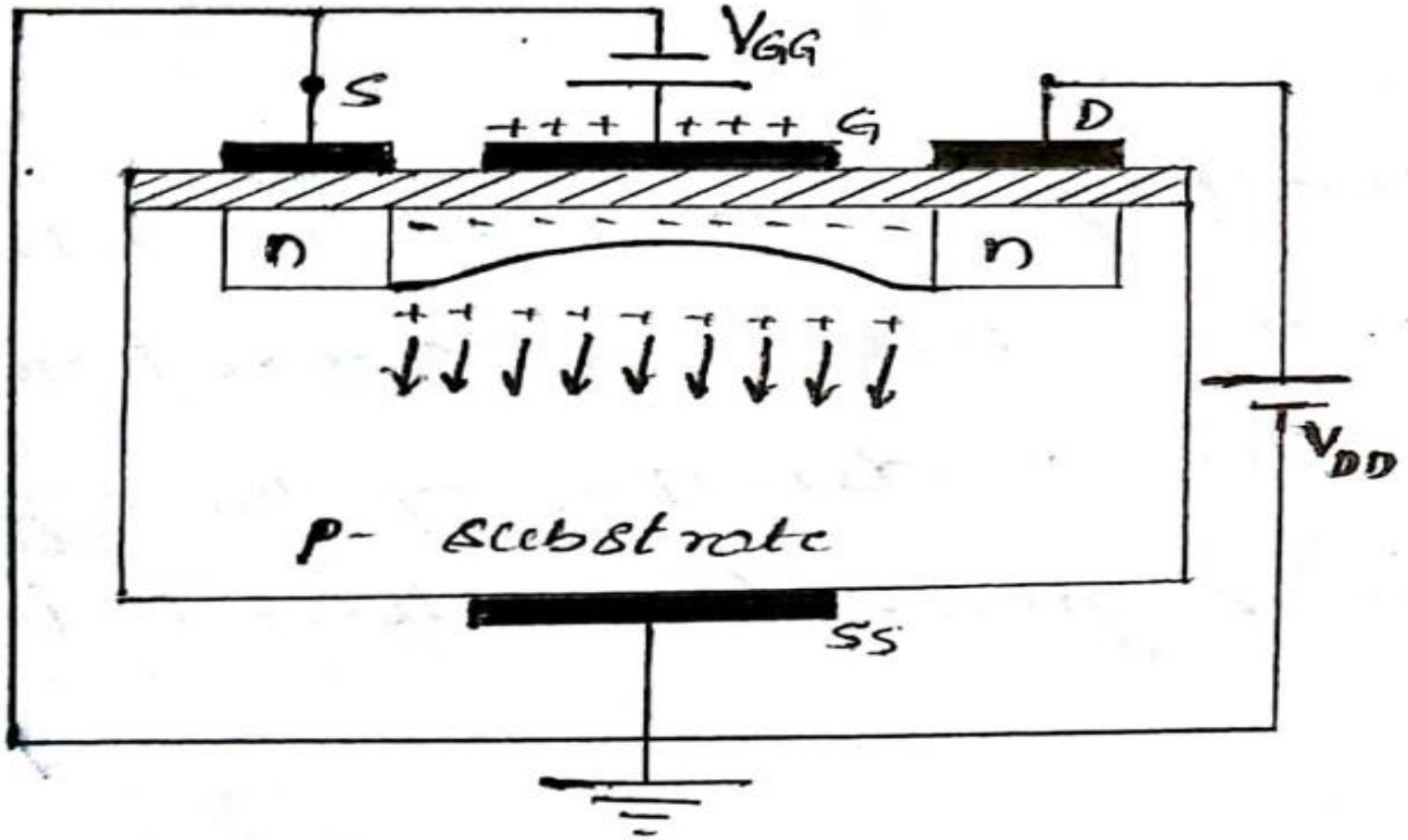
Construction:

- Consider a slab of P-type substrate which is attached with a metallic contact called as Substrate terminal(SS).
- Two N-type materials are doped in the p-type substrate which is connected through the metallic contacts, which forms the two terminals namely Source(S) and Drain(D).
- Here there is no physical cannel between the source and the drain terminals.
- The n-channel E-MOSFET is as shown in the figure.
- Dotted lines in the symbolic representation individuals the absence of channel.

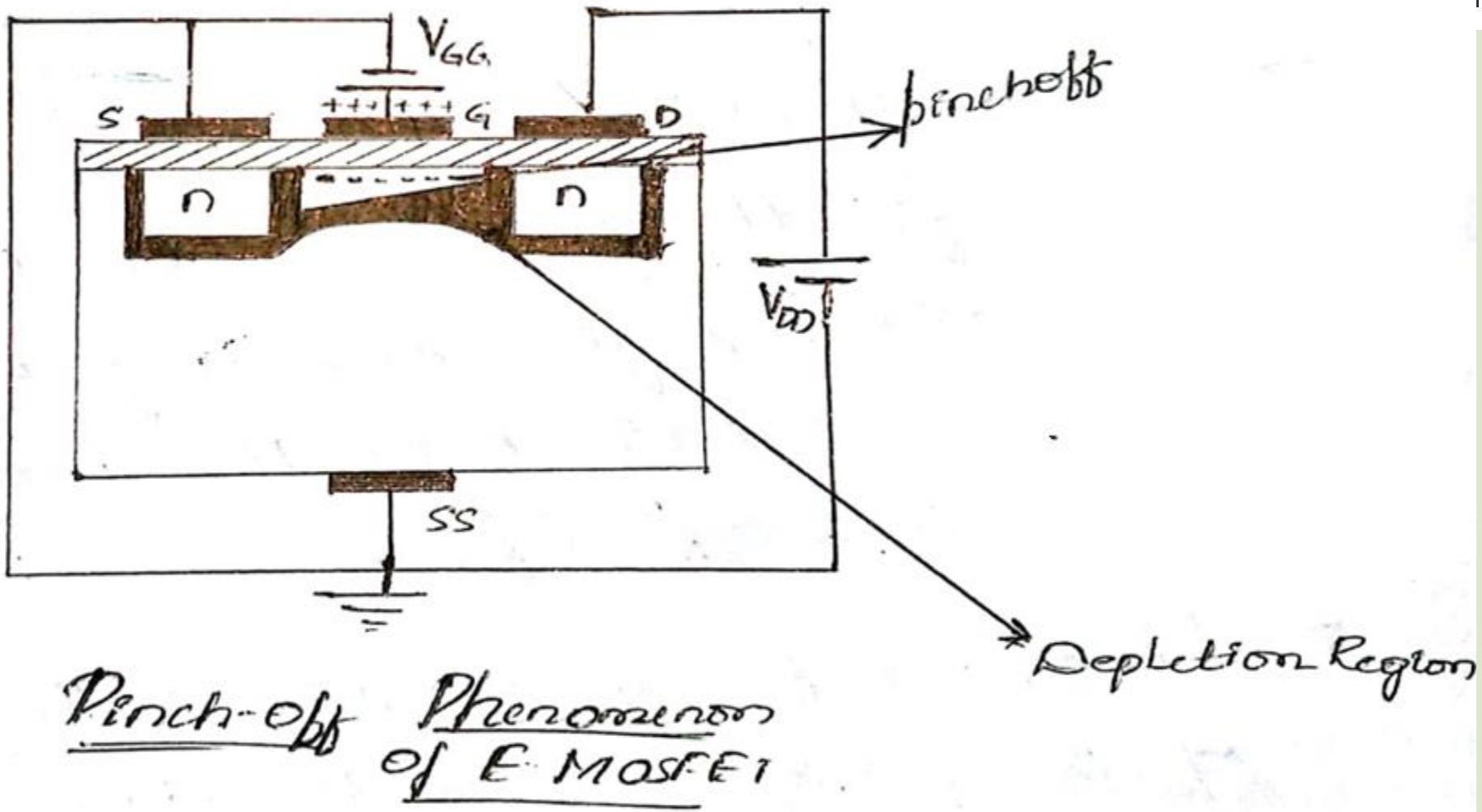
OPERATION:



OPERATION:



OPERATION:


V_{GG}
S
G
D
n
n
pinchoff
V_{DD}
SS
Depletion Region
Pinch-off Phenomenon of E-MOSFET

OPERATION:

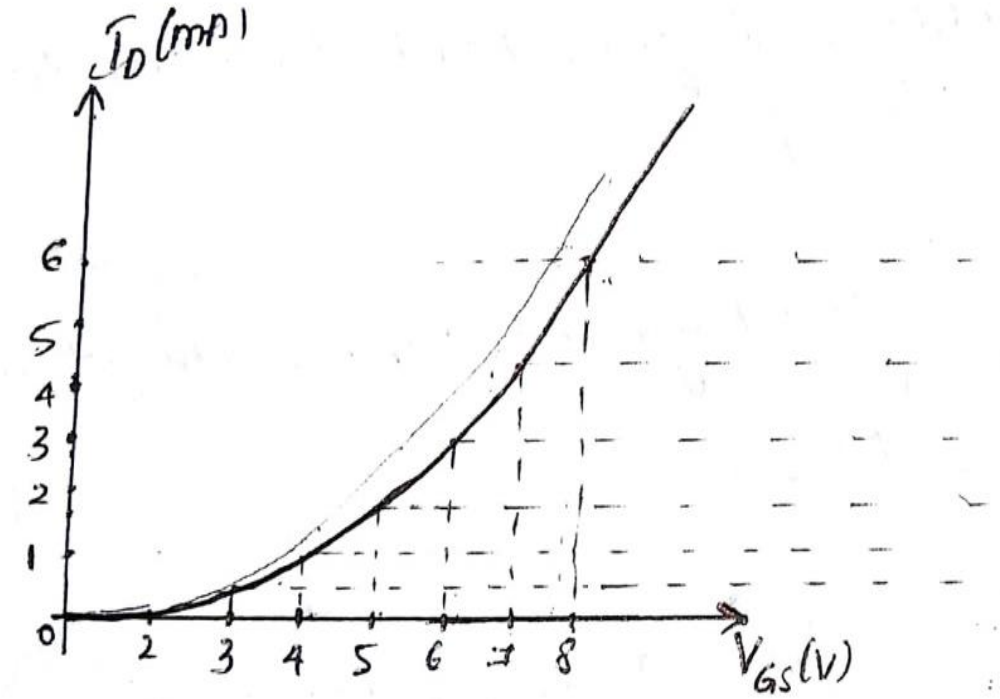
- When the gate-to-source voltage $\mathbf{V_{GS}}$ is zero and a voltage is applied between the drain and the source V_{DS} in the absence of n-channel will result in a current of effectively 0A.

- Drain current flows only when a positive voltage is applied to the gate terminal w.r.t source terminals, which induces a channel by drawing the electrons in the p-type substrate to accumulate near the surface of the SiO_2 layer.

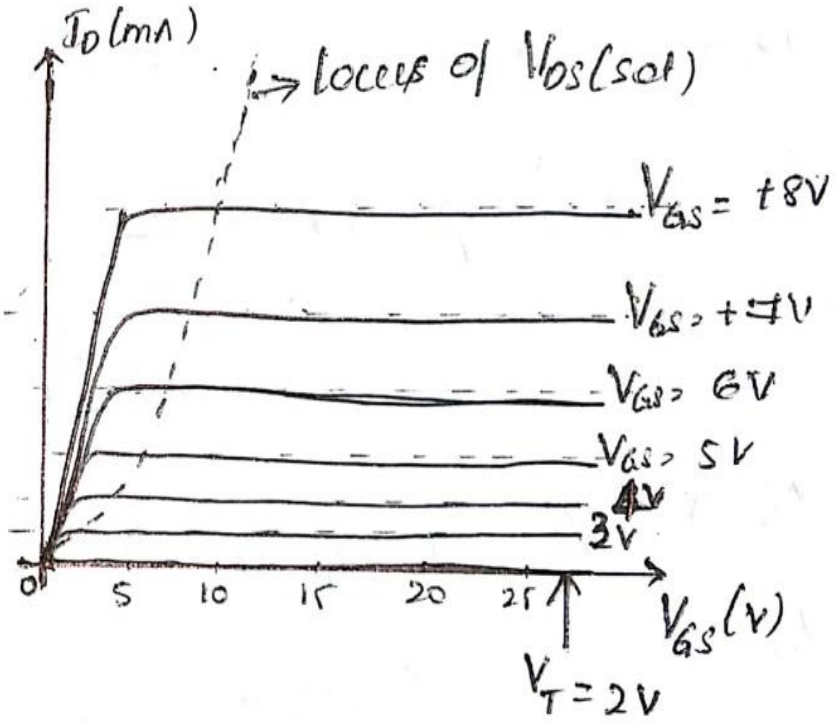
- As the value of $\mathbf{V_{GS}}$ is increased by making gate terminal more positive, more and more the electrons accumulate leading to an enhanced flow of drain current. Hence these MOSFET's are called as Enhancement MOSFET.

- The level of gate-to-source voltage **[V_{GS}]** that leads to significant flow of drain current is referred to as threshold voltage and is denoted by **V_T**.

- For fixed **V_{GS}**, if we increase the **V_{DS}**, **I_D** initially increases and gets saturated.
- Reduction in the channel width near the drain region. This effect is known as pinch-off effect.
- The value of drain-source voltage at which the drain current saturates is given by **$V_{DS\ (sat)}$**.
- From the output characteristics curve, we can observe that the **$V_{DS(sat)}$** voltage increases with the increases in the applied gate-to-source voltage.
- Relationship between the **$V_{DS(sat)}$** and **V_{GS}** is given by equation **$V_{DS(sat)} = V_{GS} - V_T$**
- Drain current is zero for the **$V_{GS} < V_T$**. For **$V_{GS} > V_T$**, the drain current is given by **$I_D = k[V_{GS} - V_T]^2$**

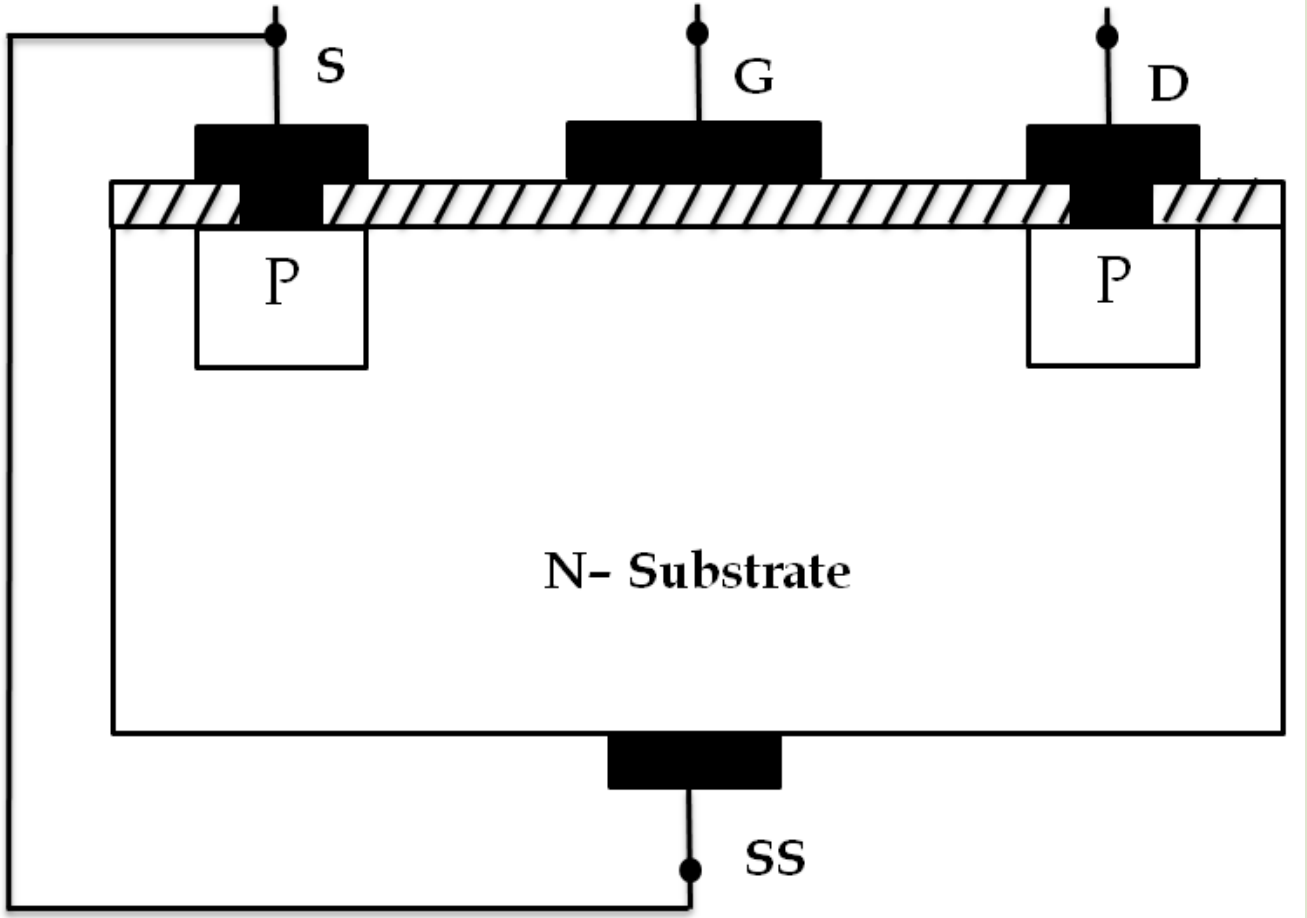


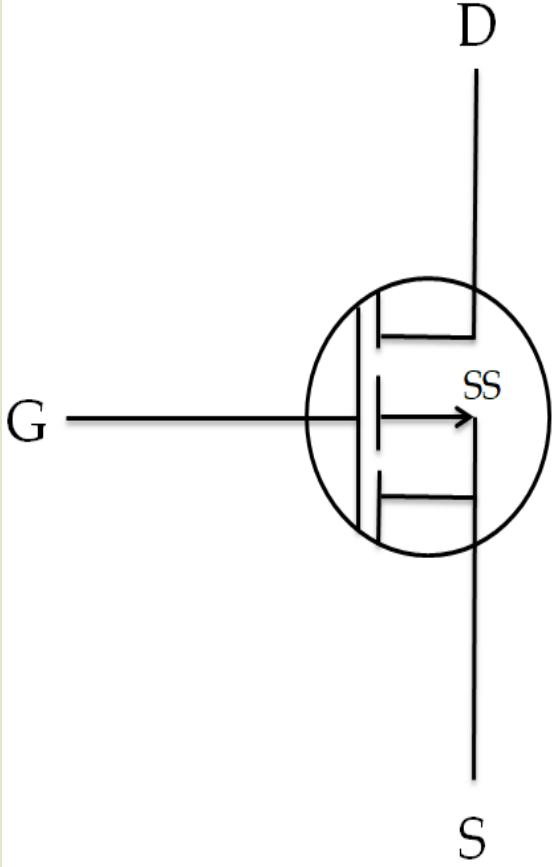
Transfer Characteristics



O/P Characteristics

P-CHANNEL E-MOSFET:



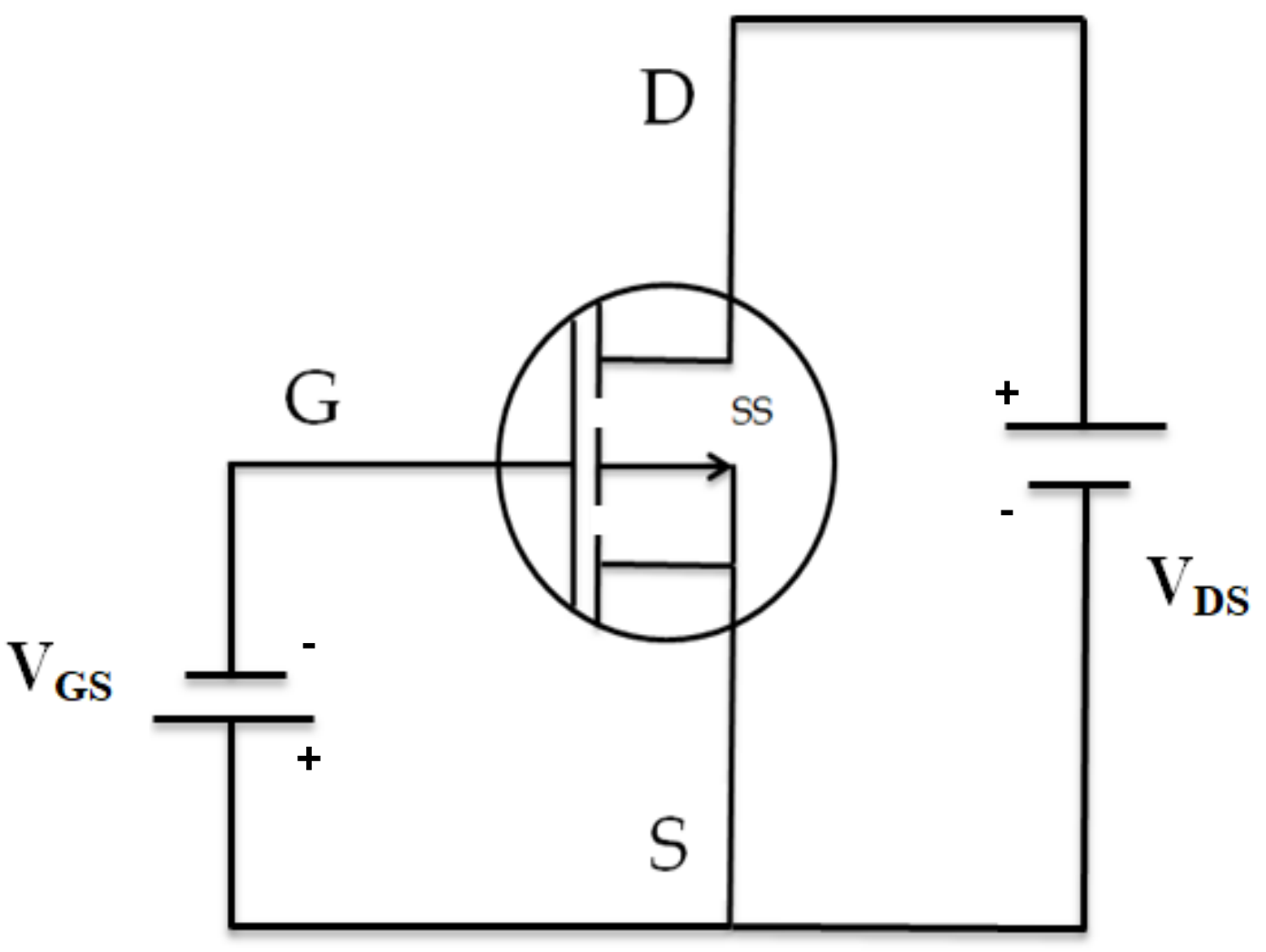


P-CHANNEL E-MOSFET:

Construction:

- Consider a slab of N-type substrate which is attached with a metallic contact called as Substrate terminal(SS).
- Two P-type materials are doped in the N-type substrate which is connected through the metallic contacts, which forms the two terminals namely Source(S) and Drain(D).
- Here there is no physical cannel between the source and the drain terminals.
- The P-channel E-MOSFET is as shown in the figure and Dotted lines in the symbolic representation individuals the absence of channel.

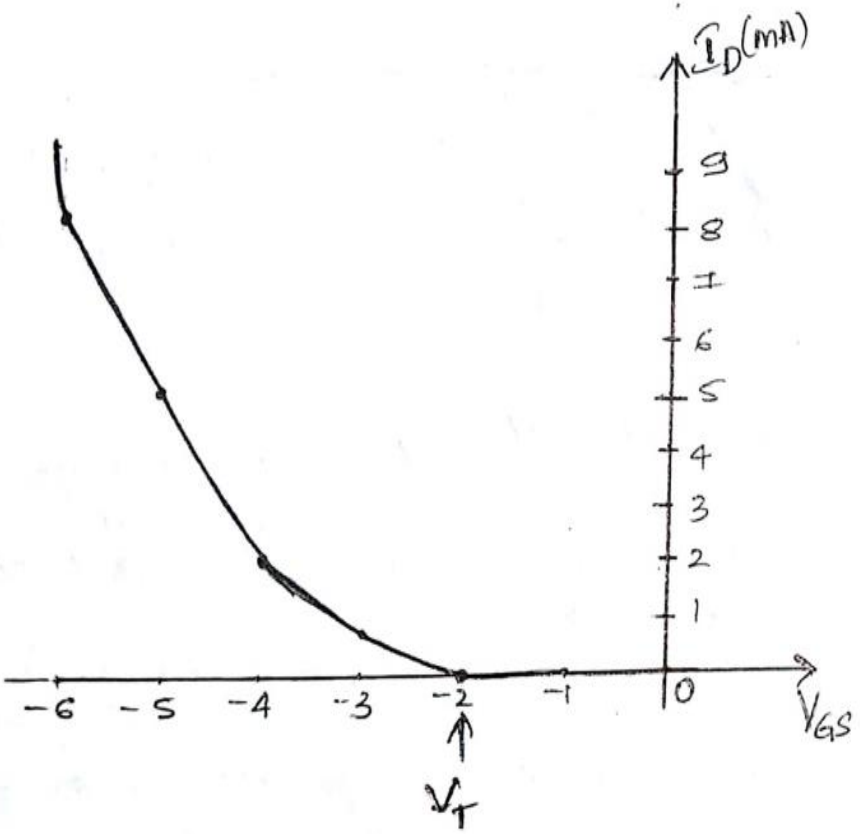
OPERATION



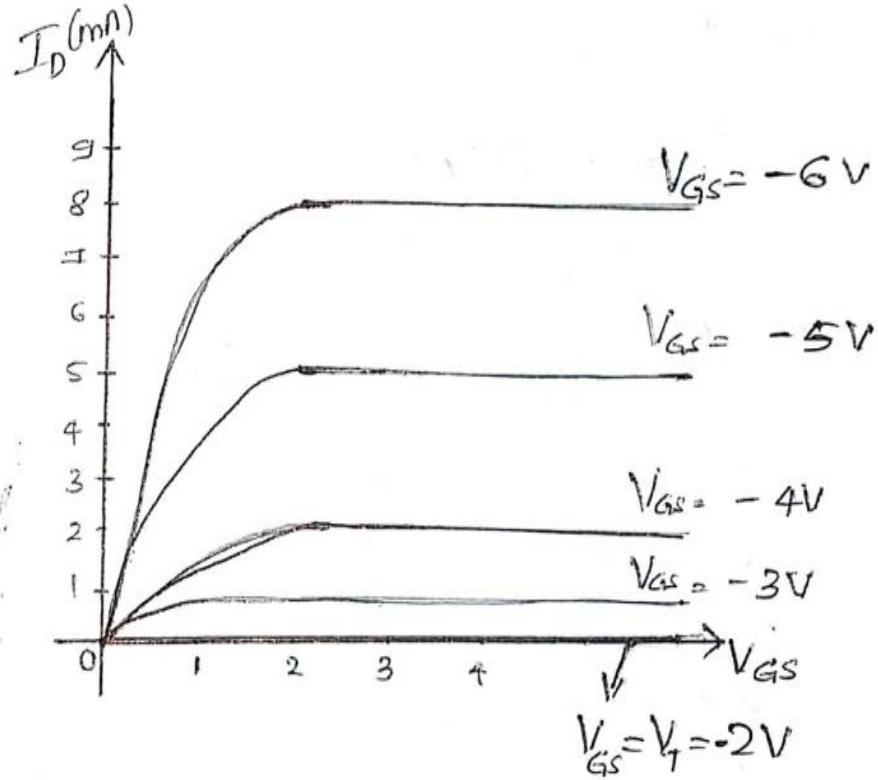
OPERATION

- When the gate-to-source voltage $\mathbf{V_{GS}}$ is zero and a voltage is applied between the drain and the source $\mathbf{V_{DS}}$ in the absence of n-channel will result in a current of effectively 0A.
- Drain current flows only when a negative voltage is applied to the gate terminal w.r.t source terminals, which induces a channel by drawing the electrons in the N-type substrate to accumulate near the surface of the SiO_2 layer.
- As the value of $\mathbf{V_{GS}}$ is increased by making gate terminal more negative, more and more the holes accumulate leading to an enhanced flow of drain current which is **reverse** to the **n-channel** DE MOSFET. Hence these MOSFET's are called as Enhancement MOSFET.
- The level of gate-to-source voltage [V_{GS}] that leads to significant flow of drain current is referred to as threshold voltage and is denoted by V_T.

- For fixed V_{GS}, if we increase the V_{DS}, I_D initially increases and gets saturated.
- Reduction in the channel width near the drain region. This effect is known as pinch-off effect.
- The value of drain-source voltage at which the drain current saturates is given by $V_{DS\ (sat)}$.
- From the output characteristics curve, we can observe that the $V_{DS(sat)}$ voltage increases with the increases in the applied gate-to-source voltage (V_{GS}).
- Relationship between the $V_{DS(sat)}$ and V_{GS} is given by equation $V_{DS(sat)} = V_{GS} - V_T$

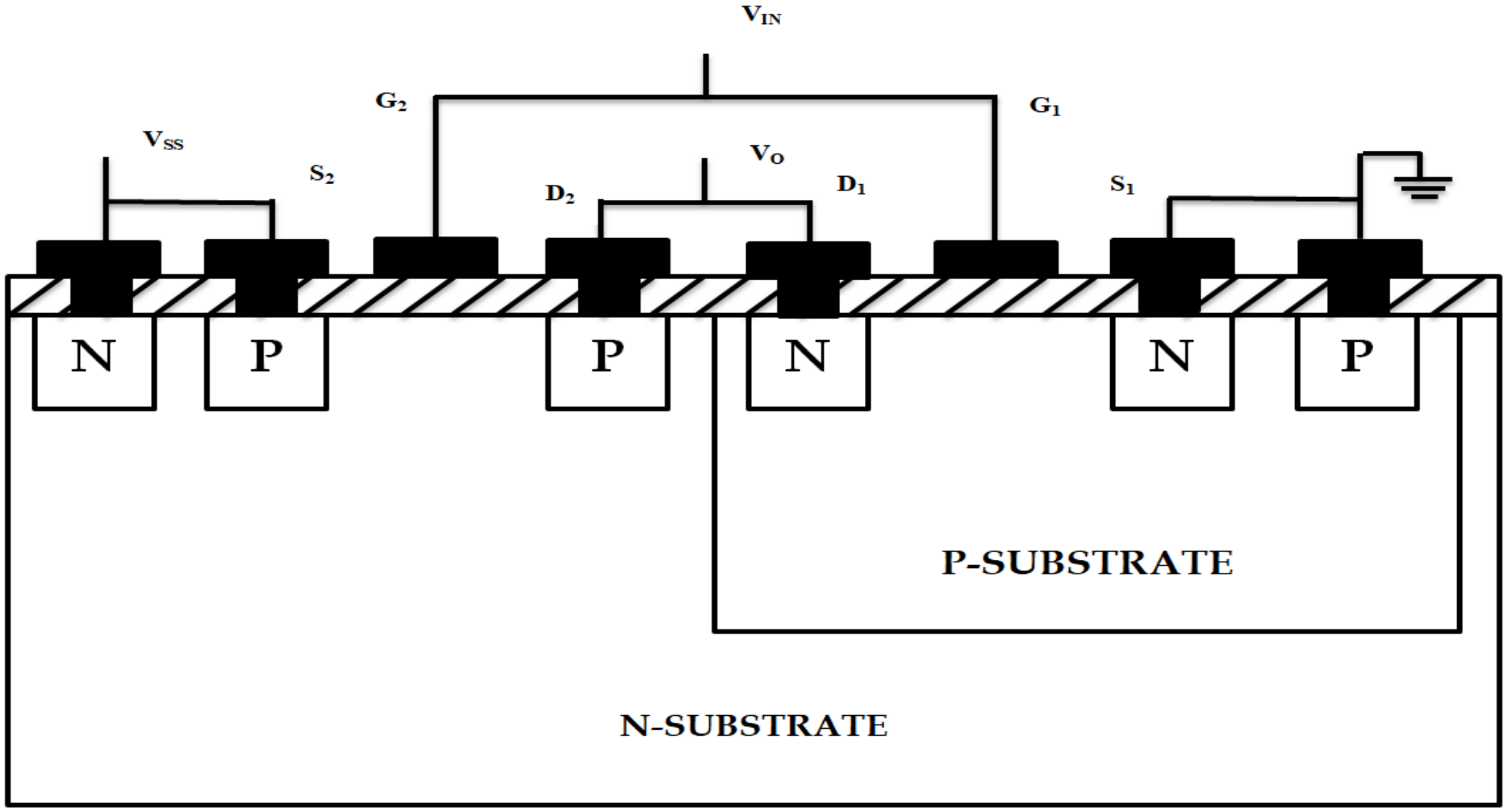


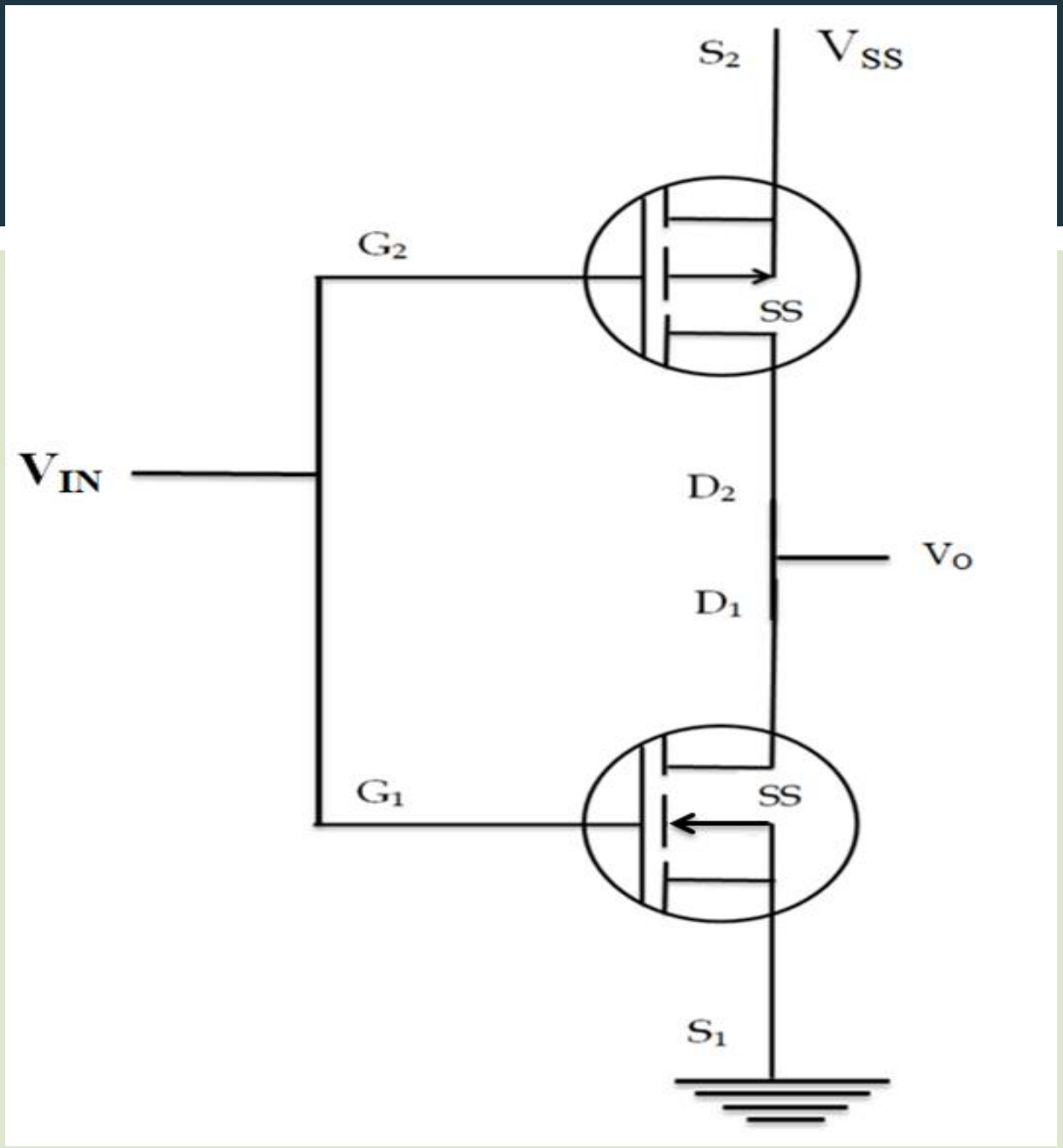
TRANSFER CHARACTERISTIC CURVE



OUTPUT CHARACTERISTIC CURVE

COMPLEMENTARY METAL OXIDE SEMICONDUCTOR [CMOS]




S2
VSS
G2
SS
VIN
D2
VO
D1
G1
SS
S1

CMOS

Construction:

- Complementary Metal Oxide Semiconductor [CMOS] are those semiconductor device in which both P-channel and the N-channel E-MOSFET are diffused onto the same chip.
- CMOS configuration has extensive application in computer logic designs.
- CMOS devices offers high input impedance, low power consumption and require for less space as compared to BJT based logic circuit.
- CMOS offers slow switching speed compared to BJT's.
- Basic inverter circuit using CMOS configuration is as shown.

- Inverter is a logic circuit that inverts the applied input signal, i.e. logic low input to logic high output and logic high input to logic low output.
- Complementary N-channel and P-channel E-MOSFET's are connected in series with gate terminals connected together to form the input terminal.
- Drain terminals are connected to form the output terminal.
- Source terminal of the P-channel MOSFET[S_2] is connected supply voltage V_{SS} and the source terminal of N-channel E-MOSFET[S_1] is connected to ground.

OPERATION

- When the input voltage $\mathbf{V_{IN}}$ is at **logic low**, the gate source voltage $\mathbf{[V_{G2S2}]}$ of the P-channel is equal to $\mathbf{-V_{SS}}$ and the MOSFET will be in the ON state, providing a low resistance path between $\mathbf{V_{SS}}$ and the output terminal.

- The gate-source voltage of N-channel is 0V $[\mathbf{V_{G1S1}}]$ and therefore it is in the OFF state, resulting high impedance between the Output terminal $[D_1]$ and ground $[S_1]$.

- *Therefore output voltage* $\boldsymbol{V_{out}}$ *is equal to supply voltage* V_{SS}. *[i.e. for logic low input* (V_{IN}*=0V), the output voltage is at logic high* ($\boldsymbol{V_O=V_{SS}}$*)*

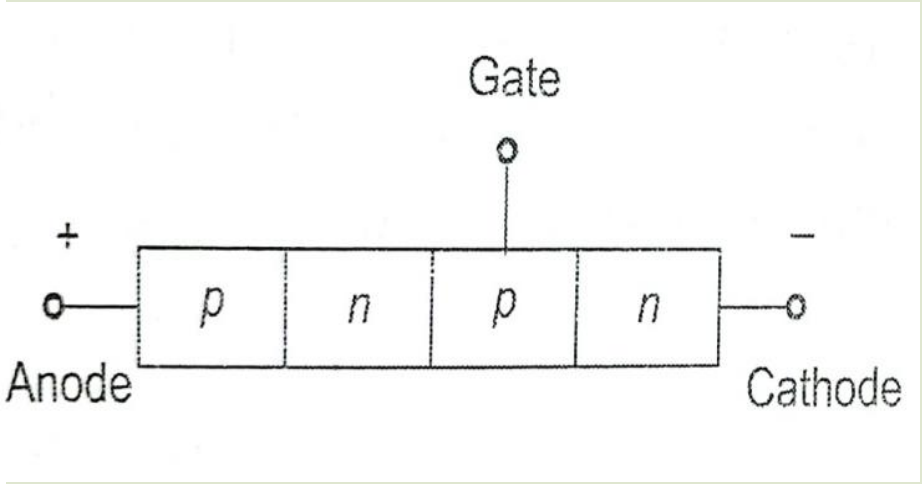
OPERATION

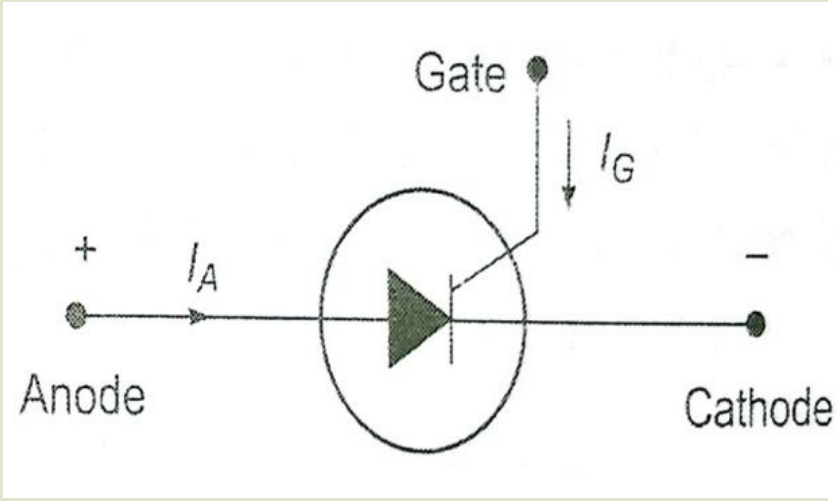
- When $\mathbf{V_{IN}}$ is at **logic high**, that is equal to supply voltage $\mathbf{V_{SS}}$, the gate to source voltage [$\mathbf{V_{G2S2}}$] of the P-channel E-MOSFET is 0V and therefore MOSFET is in OFF state.
- The gate-source voltage of N-channel is equal to supply voltage $\mathbf{V_{SS}}$ and hence it is in ON state, resulting low resistance path.
- Two MOSFET's form a voltage divider and output voltage is approaching equal to 0 V.
- *Hence logic high input results in logic low output.*

SILICON CONTROLLED RECTIFIER

- It is a four-layer device which has wide range of applications like rectifiers, regulated power supplies, dc to ac conversion (inverter), relay control, time delay circuits.

- SCR; are used to control high power of 10MW with individual rating of 2KA and 1.8KV with frequency range extended upto 50 KHz.

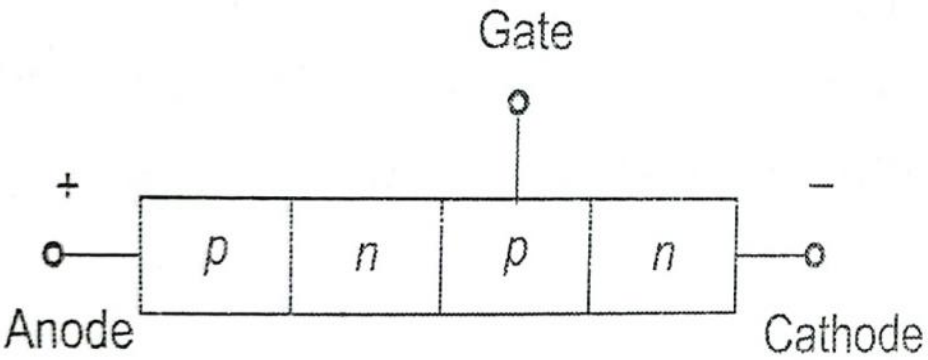




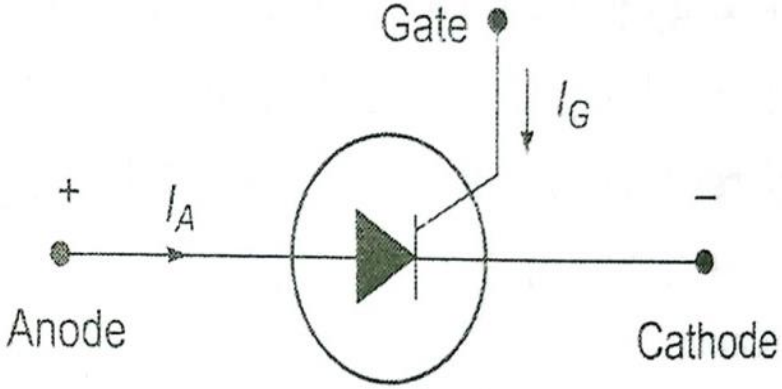
OPERATION

- The material used for SCR is silicon because of high-temperature requirement of handling large current and power.
- Its four layers is arranged as **PNPN** shown in figure (a) and the outer layers are connected to terminals to form Anode (positive terminal) and Cathode (negative terminal) and the p layer closer to the cathode terminal is connected to the Gate terminal.
- The SCR symbol is drawn in the figure (b).
- As the forward voltage is applied across the anode and cathode, no conduction takes place as the middle ***np*** junction is reverse biased.
- If a positive pulse is applied at the gate terminal, such that a current of magnitude equal to or more than I_G (turn-on) flows into the gate, the processes in the device cause it to go into the conduction.

- The forward current is offered a resistance as low as 0.01 Ω to 0.1Ω.
- Because of regenerative action, removing the gate current does not cause the device to turn off.
- The dynamic resistance of SCR is as high as 100 K Ω or more.



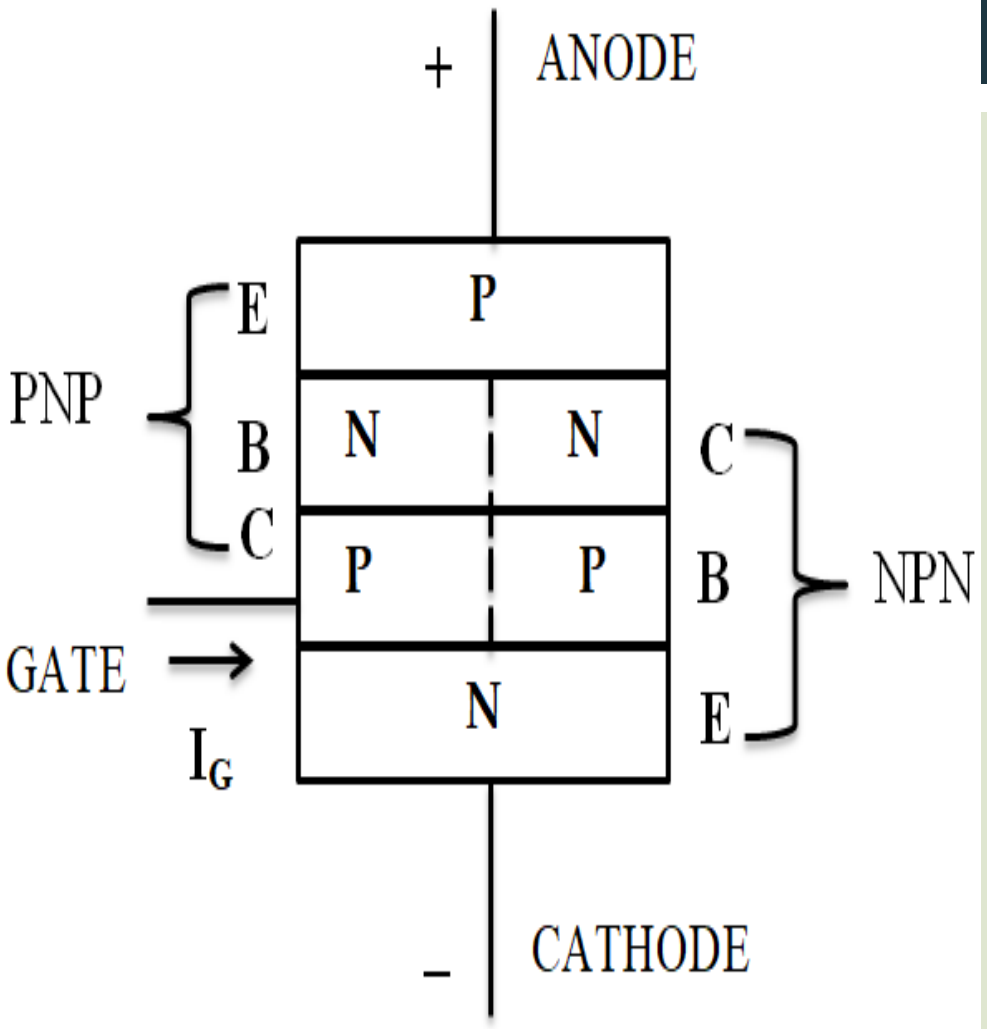
(a) Basic layout

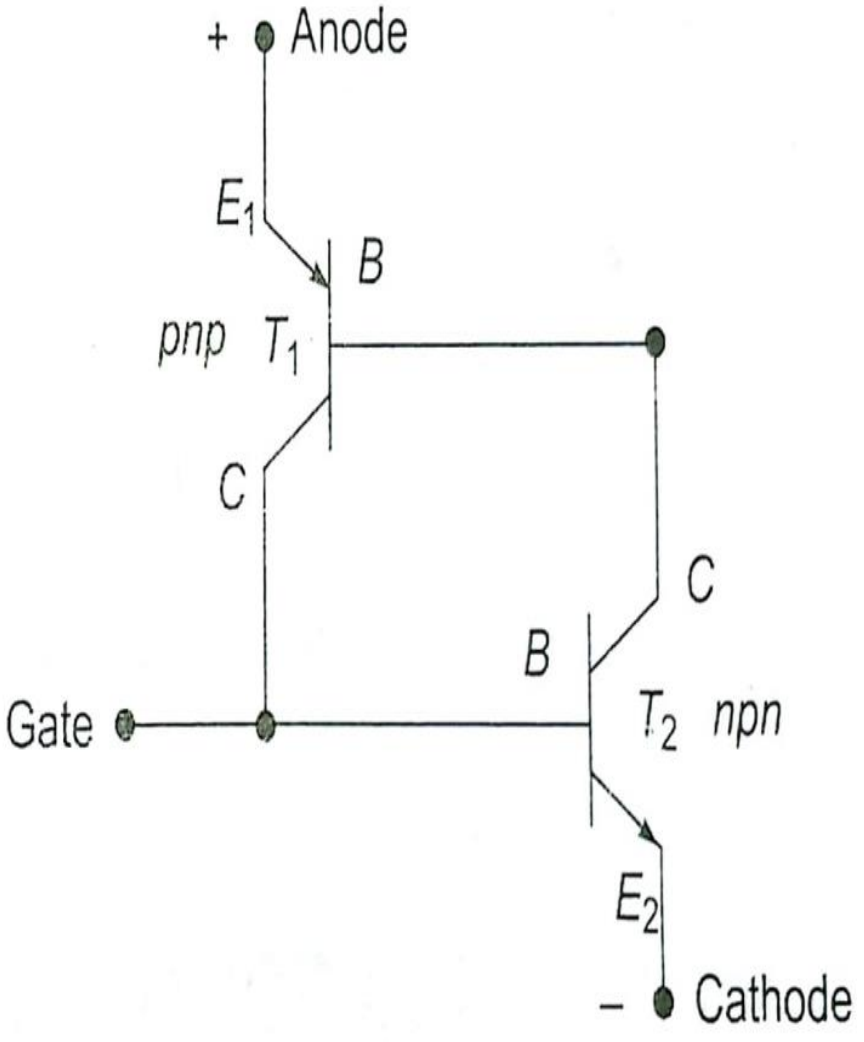


(b) Symbol

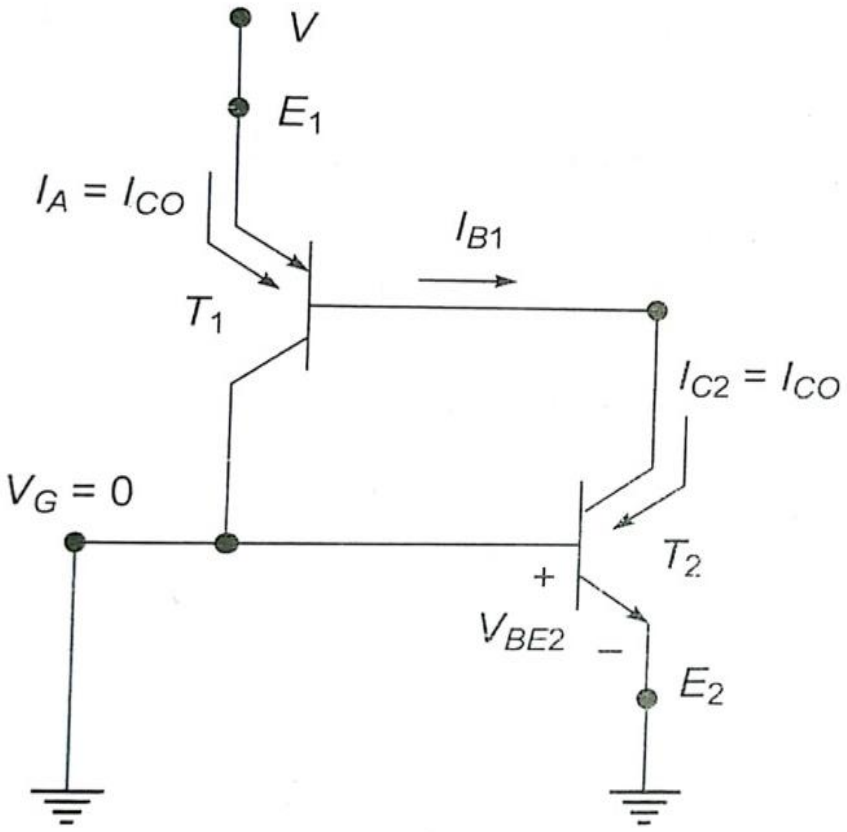
TWO TRANSISTOR MODEL OF SCR

- The cross-sectional view of an SCR with the four layers is drawn as shown below in figure (a).
- The middle n and p layers can be imagined to be subdivided into two halves, as shown by the dotted line.
- Now it can be recognised that the device comprises one ***PNP*** and one ***NPN*** transistor.
- Since there is connectivity between two halves of each of these layers, the **Base** of the ***PNP*** is connected to the **Collector** of ***NPN*** and the **Collector** of ***PNP*** is connected to the **Base** of the ***NPN***, while the ***Gate*** is connected to the **Base** of ***NPN***.
- The corresponding two transistor model equivalent circuit is as shown below in the figure (b).

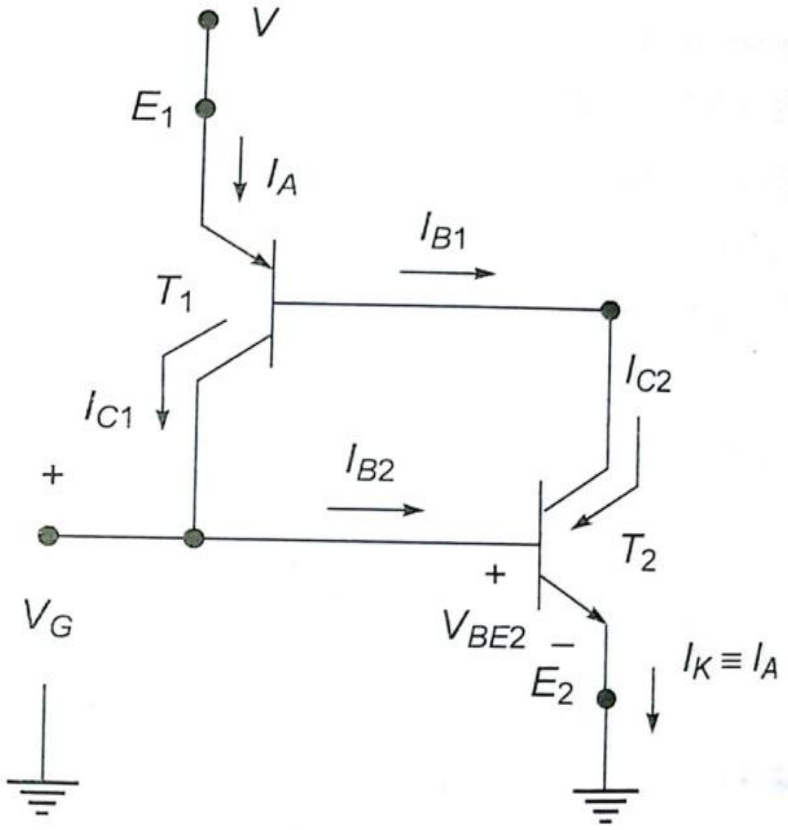

+
ANODE
E
P
PNP
B
N
N
C
C
P
P
B
NPN
GATE
N
E
I_G
–
CATHODE


+
Anode
E_1
B
pnp
T_1
C
C
B
Gate
T_2
npn
E_2
–
Cathode

SWITCHING ACTION OF SCR



(a) With $V_G = 0$



(b) With voltage V_G applied

- Let a positive voltage V be applied to the anode (E_1) and the cathode (E_2) and gate (G) be both grounded as shown in figure (a).
- As $\mathbf{V_G = V_{BE2} = 0}$, the transistor $\mathbf{T_2}$ is in 'OFF' state.

- It means that CB-junction of $\mathbf{T_2}$, through EB-junction of $\mathbf{T_1}$, is reverse biased.
- Therefore, $\mathbf{I_{B1} = I_{CO}}$ (minority carrier current) is too small to 'turn-on' $\mathbf{T_1}$.
- Thus both $\mathbf{T_1}$ and $\mathbf{T_2}$ are 'OFF' and so anode current $\boldsymbol{I_A = I_{B1} = I_{CO}}$ is of negligible order.
- It means that SCR is in 'turn-off' state, that is the switch between anode (E_1) and cathode (E_2) is open.
- Now, let a voltage $+V_G$ be applied at the gate as shown in figure (b), as $\mathbf{V_{BE2} = V_G}$, on making $\mathbf{V_G}$ sufficiently large, $\mathbf{I_{B2}}$ will cause T_2 to turn on and the collector current I_{C2} becomes large.

- As $\mathbf{I_{B1} = I_{C2}}$, T_2 turns on causing a large collector current $\mathbf{I_{C1}}$ $\mathbf{(I_A = I_{C1})}$ to flow.
- This in turn, increase I_{B2} causing a regenerative action to set in.
- The result is that the SCR is turned on, that is, the switch between the anode (E_1) and cathode (E_2) is closed (turn-on).
- The current $\mathbf{I_A}$ must be limited by the external circuit, say a series resistance between the source and E_1.
- The turn on time of an SCR is typically **0.1 to 1µs**.

TURNING OFF SCR

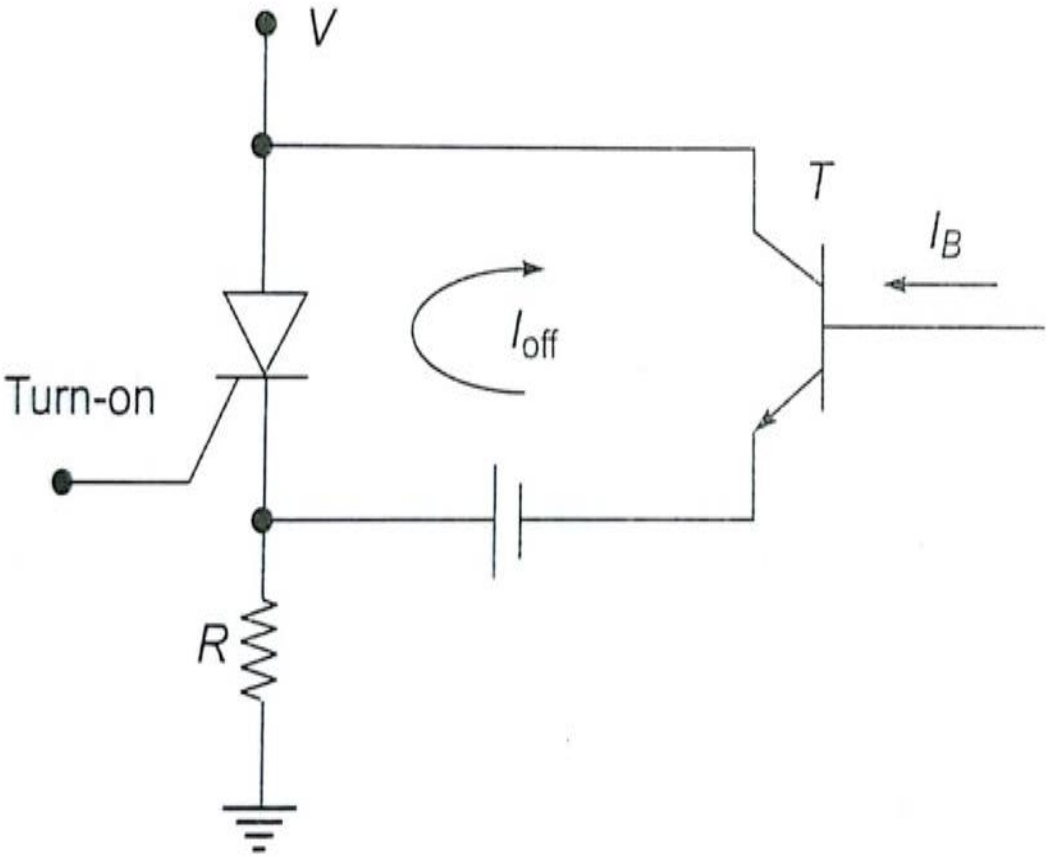
When the SCR is in conduction mode, the gate is ineffective in turning it off. The turn-off mechanism is called Commutation and it can be achieved in two ways explained below.

Natural Commutation:

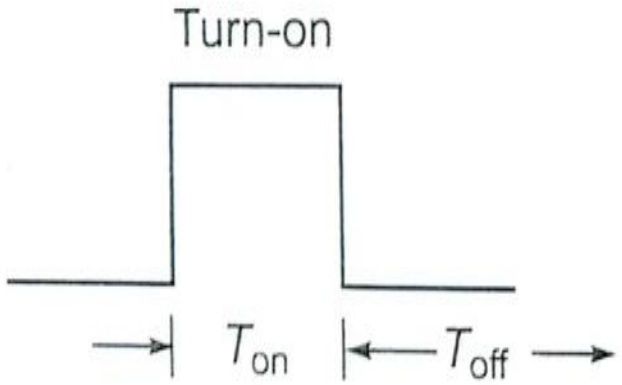
- When the source that feeds the current to anode of SCR is such that it naturally passes through zero, the SCR turns off at the current zero. This is the case when the SCR is fed from the AC sources. In this situation, the commutation is also known as *line commutation*.

Forced Commutation:

- In this method of commutation, the current through the SCR is forced to become zero by passing a current through it in opposite direction from an independent circuit.

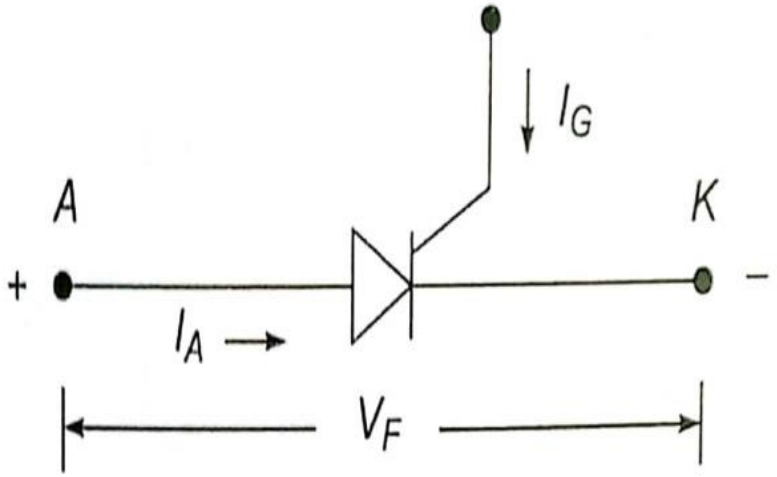


(a) Circuit

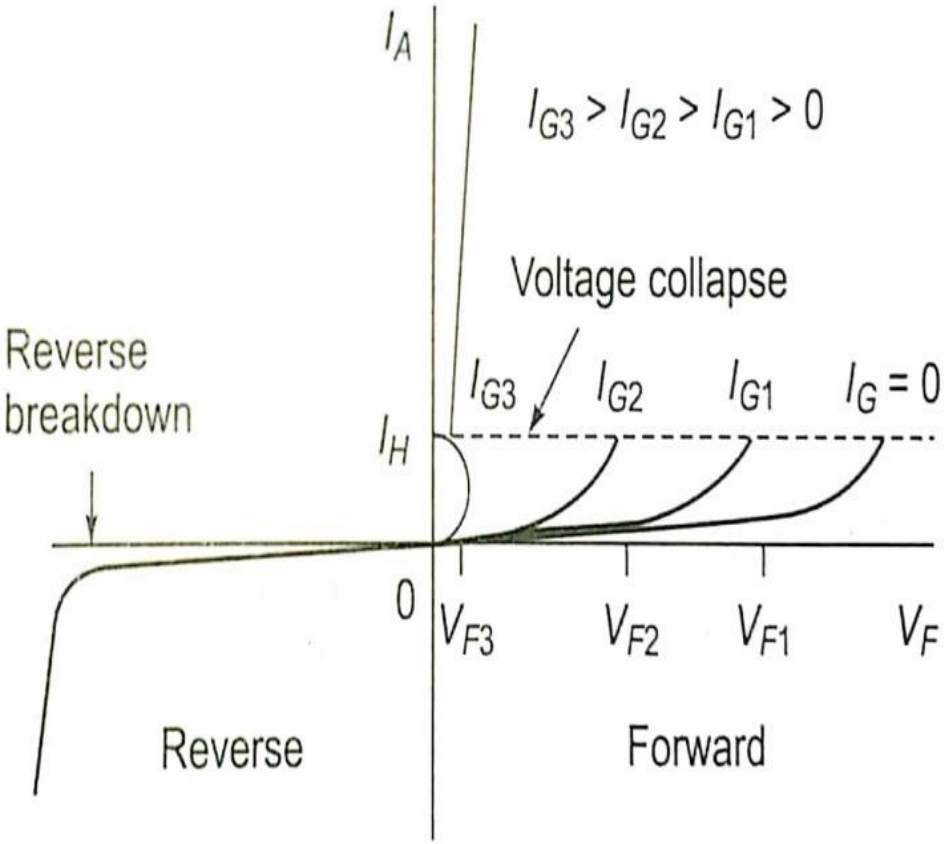


(b) Output waveform

SCR CHARACTERISTICS



(a) Symbol



(b) I-V characteristics

- The symbol and I-V characteristics of SCR are given below. Various voltages and current ratings of SCR are described below:

- ***Forward Breakover Voltage V_F (BR)***: It is the voltage at which for a given I_G, the SCR enters into conduction mode. From the graph we can see that, this voltage reduces as I_G increases. V_F (BR) has dependence on the circuit connection between G and K terminals.

- ***Holding Current I_H***: It is the value of the current below which SCR switches from conduction state to forward blocking region of specified conditions.

- Forward and Reverse blocking regions are those regions in which the SCR is open circuited and no current flows from anode to cathode.

- Reverse breakdown voltage corresponds to Zener or Avalanche region of a diode.

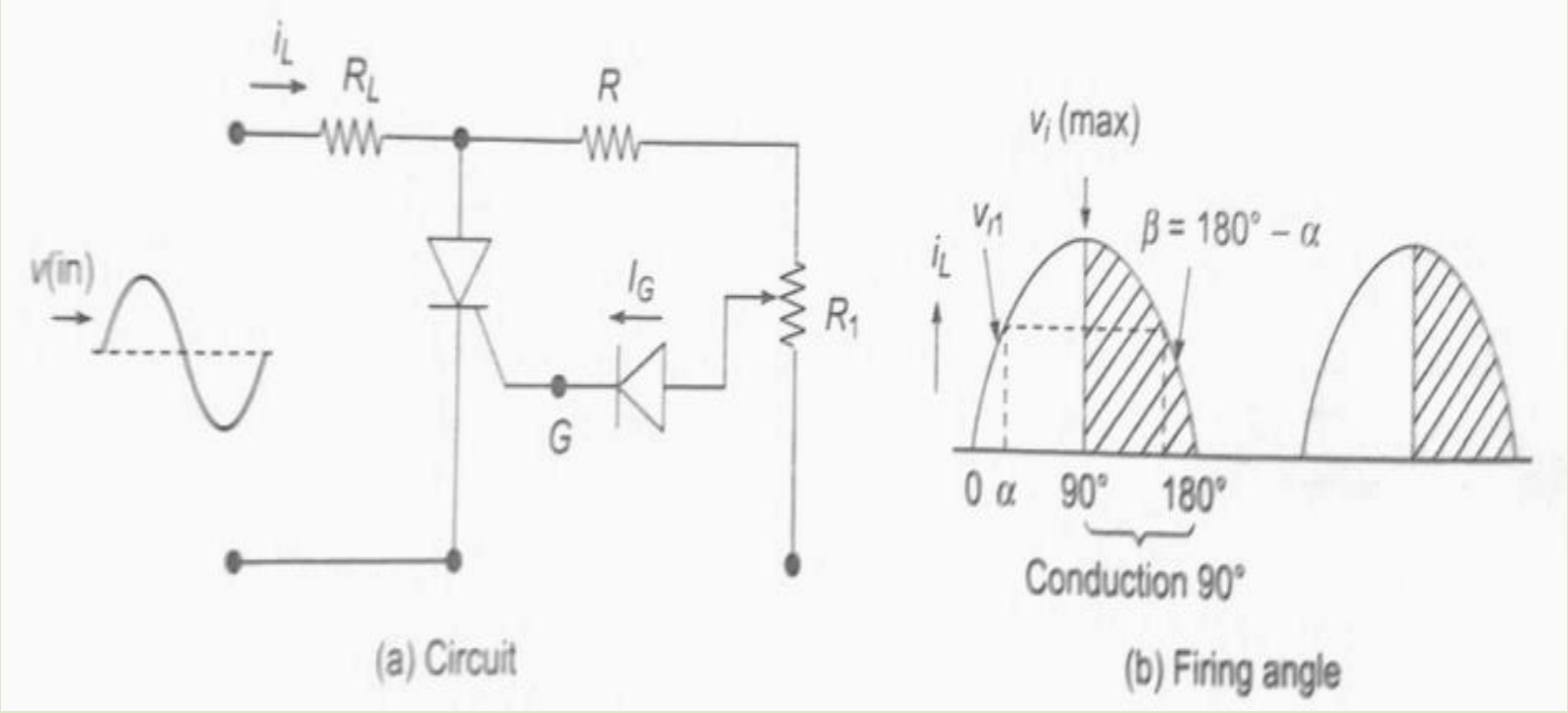
SCR APPLICATIONS

- One of the applications of SCR we are studying is, Variable Resistance Phase controlled.
- A variable-resistance phase control circuit is as shown below in figure (a).
- The SCR gate current is controlled through the resistance R and the variable resistance R_1.
- Let the RG be adjusted to high value so that even at the peak value v_i positive, $\mathbf{I_G} < \mathbf{I_{G(turn\ on)}}$ and no conduction takes place.
- As $\mathbf{R_1}$ is reduced, $\mathbf{I_G}$ rises to turn-on value at the particular angle (time) of v_i.
- The conduction then begins and continues till $\mathbf{V_I}$ reaches zero(180^o).
- Varying $\mathbf{R_1}$ allows adjusting the SCR firing angle from 0^0 to 90^0 as shown in the figure (b) below.

- At $\mathbf{R_1}$, corresponding to the firing angle of $\mathbf{90^0}$, $\mathbf{V_I = V_{I(max)}}$. If R1 is adjusted for firing at α, the firing will take place at angle $\boldsymbol{\alpha < 90^0}$ but not at angle but not at angle $\boldsymbol{\beta = (180^0 - \alpha) > 90^0}$ as the angle α is reached earlier in time on the $\mathbf{V_I}$ wave.

- So the operation of this circuit is known as *half-wave, variable-resistance phase control.*

- Thus $\mathbf{I_{L(DC)}}$ can be adjusted to the maximum value at 0^0 to the minimum value at 90^0.



PROBLEMS

For the given drain characteristics of JFET, I_{DSS} = 8mA and V_P = – 4V. Using Shockley's equation, find the value of I_D for V_{GS} = – 1V and V_{GS} = – 2V .

Given: I_{DSS} = 8mA; V_P = – 4V

We know that,

$$I_D = I_{DSS} * \left[1 - \frac{V_{GS}}{V_P}\right]^2$$

At V_{GS} = – 1 V

$$I_D = 8m * \left[1 - \frac{-1}{-4}\right]^2$$

$$= 8^* \left[\frac{3}{4}\right]^2 \text{mA}$$

$$= 4.5 \text{ mA}$$

At V_{GS} = – 2 V

$$I_D = 8m * \left[1 - \frac{2}{4}\right]^2$$

$$= 8^* \left[\frac{1}{2}\right]^2 \text{mA}$$

$$= 2 \text{ mA}$$

At Q-point of JFET, I_{OQ} = 3.5mA, and V_{GS} = – 3V. Determine I_{DSS} if V_P = – 6V

Given: I_D = 3.5mA; V_{GS} = – 3V; V_P = – 6V

We know that,

$$I_D = I_{DSS} * \left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$3.5m = I_{DSS} * \left[1 - \frac{3}{6}\right]^2$$

$$3.5\text{m} = I_{DSS} * \left[\frac{1}{2}\right]^2$$

$$\boldsymbol{I_{DSS} = 14\ \text{mA}}$$

For JFET, I_{DSS} = 6mA and V_P = – 4.5V.

i) Determine I_D at V_{GS} = – 2V and –4V.

ii) Determine V_{GS} at I_D = 3mA and 5.5mA.

Given: I_{DSS} = 6mA; V_P = – 4.5V

We know that, $I_D = I_{DSS} * \left[1 - \frac{V_{GS}}{V_P}\right]^2$

At V_{GS} =– 2V

$$I_D = I_{DSS} * \left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$I_D = 6m * \left[1 - \frac{2}{4.5}\right]^2 =$ **1.85mA**

At V_{GS} =– 4V

$$I_D = I_{DSS} * \left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$I_D = 6m * \left[1 - \frac{4}{4.5}\right]^2 =$ **0.074mA**

At I_D =3mA

$$3 = 6 * \left[1 - \frac{V_{GS}}{-4.5}\right]^2$$

$0.5 = (1 + 0.22V_{GS})^2$

$1 + 0.22V_{GS} = \pm 0.707$

$0.22V_{GS} = -1.707; -0.293$

V_{GS} = – 1.32V

V_{GS} = – 7.73V > V_P Rejected

At I_D =5.5mA

$1 + 0.22V_{GS} = \pm 0.917$

$0.22V_{GS} = -0.047; -1.957$

V_{GS} = – 0.194V

For a depletion-type MOSFET, I_D = 10mA, at V_{GS} = – 1V. Determine V_P if I_{DSS} = 15mA.

Given: I_D = 10mA; V_{GS} = – 1V; I_{DSS} = 15mA

We know that,

$$I_D = I_{DSS} * \left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$10 = 15 * \left[1 - \frac{-1}{V_P}\right]^2$$

$$\boldsymbol{V_P = -5.45V}$$

For a DMOSFET, I_D = 4.5mA, at V_{GS} = – 2V. Determine I_{DSS} if, V_P = – 5V.

Given: I_D = 4.5mA; V_{GS} = – 2V; V_P= – 5V

We know that,

$$I_D = I_{DSS} * \left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$4.5m = I_{DSS} * \left[1 - \frac{-2}{-5}\right]^2$$

$$\boldsymbol{I_{DSS} = 12.5mA}$$

For a EMOSFET, $V_T = 4V$, $I_{D(ON)} = 4mA$, $V_{GS(ON)} = 6V$
Determine to write general expression for I_D and find I_D for $V_{GS} = 8V$

Given: $V_T = 4V$, $I_{D(ON)} = 4mA$, $V_{GS(ON)} = 6V$,

At $V_{GS} = 8V$, $I_D = ?$

We know that,

$$\mathbf{I_D = k(V_{GS} - V_T)^2}$$

$$k = \frac{I_{D(ON)}}{\left(V_{GS(ON)} - VT\right)^2}$$

$$k = 1*10^{-3}\ A/V^2$$

At $V_{GS} = 8V$

$$\mathbf{I_D = k(V_{GS} - V_T)^2}$$

$$\boldsymbol{I_D = 16mA}$$

For an EMOSFET, $k = 0.45*10^{-3}\ A/V^2$, $I_{D(ON)} = 3.5mA$, $V_{GS(ON)} = 4.5V$. Determine V_T.

Given:

$k = 0.45*10^{-3}\ A/V^2$, $I_{D(ON)} = 3.5mA$, $V_{GS(ON)} = 4.5V$.

We know that,

$$\mathbf{I_D = k(V_{GS} - V_T)^2}$$

$$\mathbf{3.5} = 0.45*(4.5 - V_T)^2$$

$$\boldsymbol{V_T = -1.71V}$$

THANK YOU

OPERATIONAL AMPLIFIERS AND APPLICATIONS

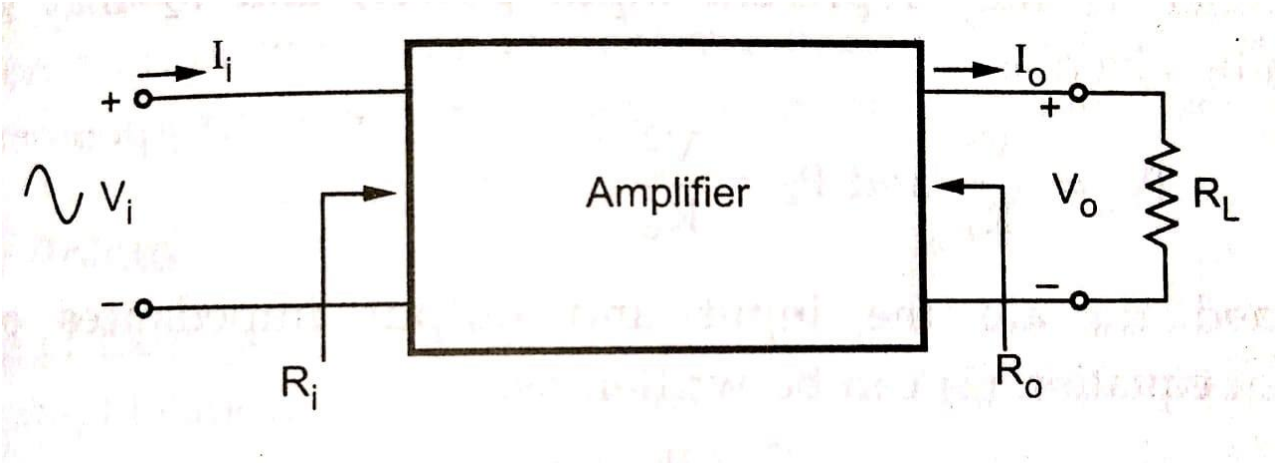
Module – 3

Presented by
Lakshmi D L
Asst. prof., Dept. of ECE
BGSIT, BG Nagara

Amplifiers

- An amplifier is an electronic circuit that amplifies small input signal without any distortion.
- An amplifier is used to increase the signal level; i.e. to get a large signal output from a small signal input.
- The ratio of output quantity to input quantity is called gain of the amplifier.
- Thus, the ratio of output voltage to input voltage will be the voltage gain of the amplifier, usually denoted by Av.
- Similarly, the ratio of output current to input current will be the current gain of the amplifier, usually denoted by Ai.
- An ideal amplifier provides as large a voltage gain and current gain, as practicable.
- The other two parameters of the amplifier are its input resistance, Ri, and the output resistance Ro.

- The input resistance is the resistance seen looking into amplifier input terminals.
- The output resistance is the resistance between output terminals looking back into the amplifier with input signal voltage source short circuited and the output terminals open circuited.
- The basic parameters of the amplifier are illustrated in fig.

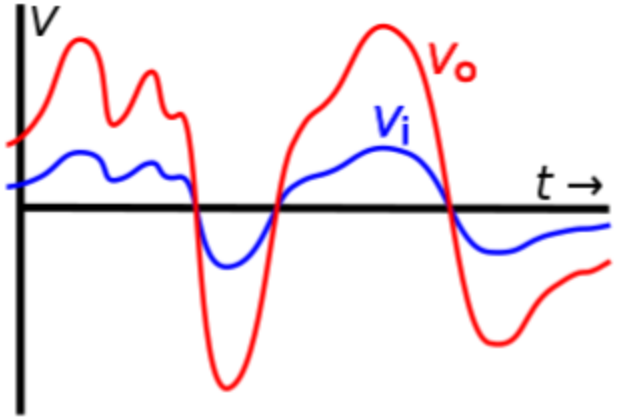


- $A_I = \frac{I_o}{I_i}$
- $A_V = \frac{V_o}{V_i} = \frac{I_o R_L}{I_i R_I}$

$$A_V = A_I \frac{R_L}{R_I}$$

Since, Power = Voltage X Current

Power Gain = Voltage Gain X Current Gain



Amplification means increasing the amplitude (voltage or current) of a time-varying signal by a given factor, as shown here. The graph shows the input $v_i(t)$ *(blue)* and output voltage $v_o(t)$ *(red)* of an ideal linear amplifier with an arbitrary signal applied as input. In this example the amplifier has a *voltage gain* of 3; that is at any instant $v_o = 3v_i$

A 100 watt stereo audio amplifier used in home component audio systems in the 1970s.

Introduction to Op-amp

- An operational amplifier or OP-AMP is a direct coupled multistage voltage amplifier with an extremely high gain.

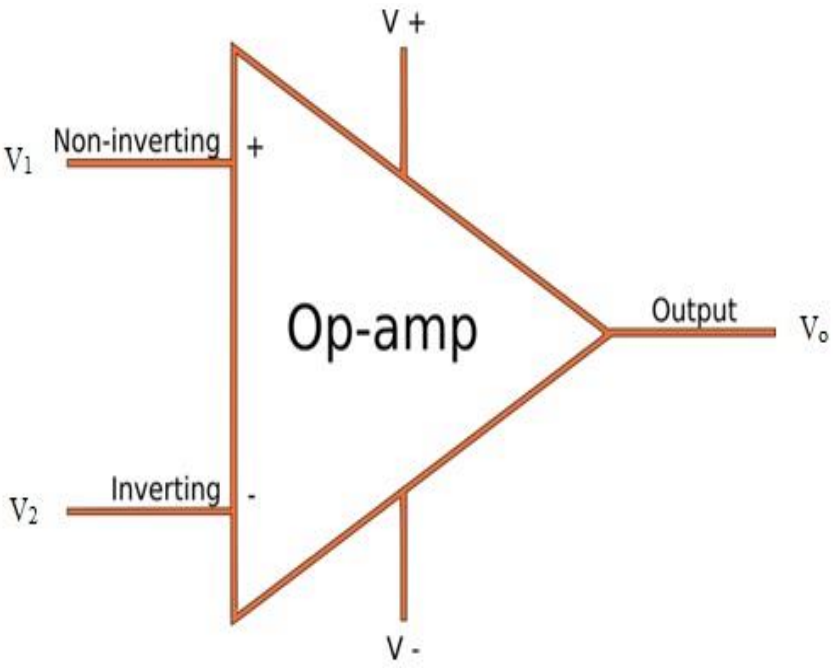
- It has very high input impedance and very low output impedance.

- The early Op-amps were mainly used for performing mathematical operations such as addition, subtraction, multiplication, integration and differentiation.

  Hence this acquired the name **Operational Amplifier(OP-AMP).**

Circuit symbol of an Op-amp

- In fig 1,
- V_1= voltage at the non-inverting input
- V_2= voltage at the inverting amplifier
- V_o= output voltage
- Voltage applied to the non-inverting input produces an in-phase or same polarity voltage at the output.
- Voltage applied to the inverting input produces an out-of phase or opposite polarity voltage at the output.
- The output voltage denoted by V_o is proportional to the difference between the input voltages
- $V_o = A (V_1 - V_2)$
- Where, A is the voltage gain.
- Hence, Op-amp is basically a **differential** or **difference amplifier**.



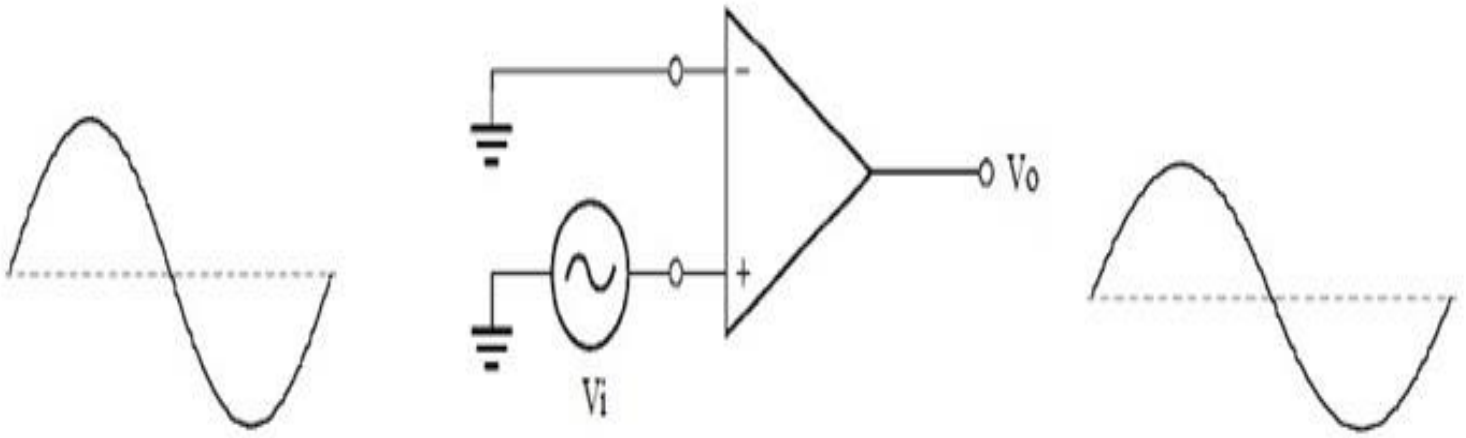
Op-amp input modes

- Based on input modes, Op-amps are classified as

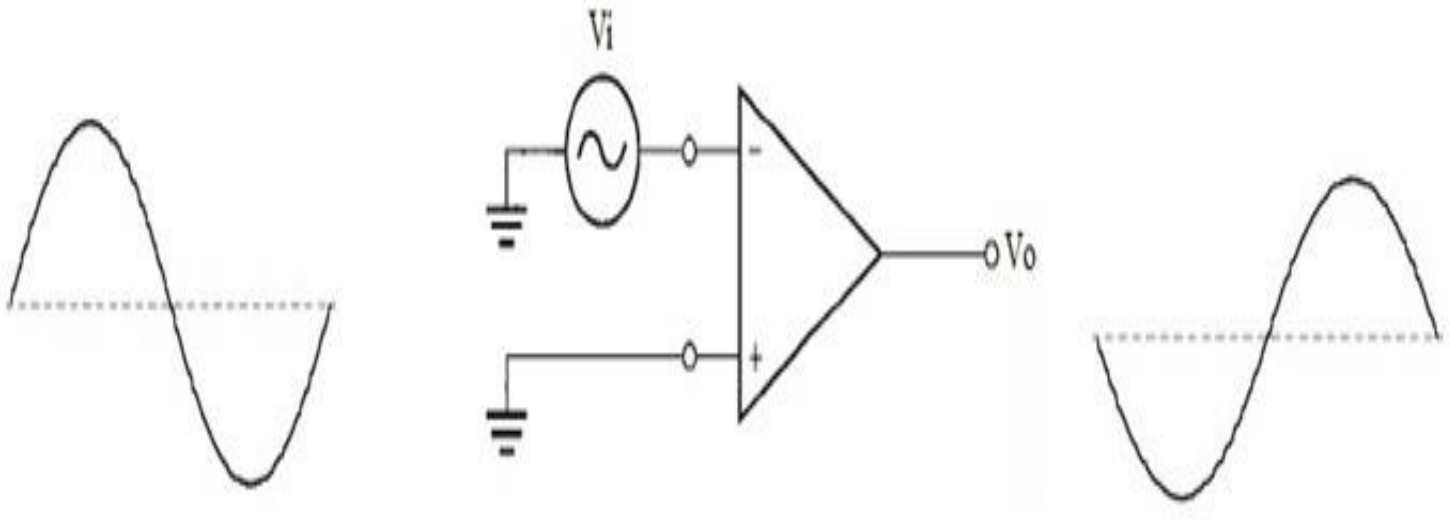
1. Single Ended input
2. Double Ended input (Differential mode)
3. Common mode operation

Single Ended Mode:

- Single ended input operation results when the input signal is connected to one input with the other input terminal connected to ground.
- Figure below shows the input is applied to Non-inverting terminal, connecting inverting terminal to ground, which results in an output having the same polarity as the input signal.

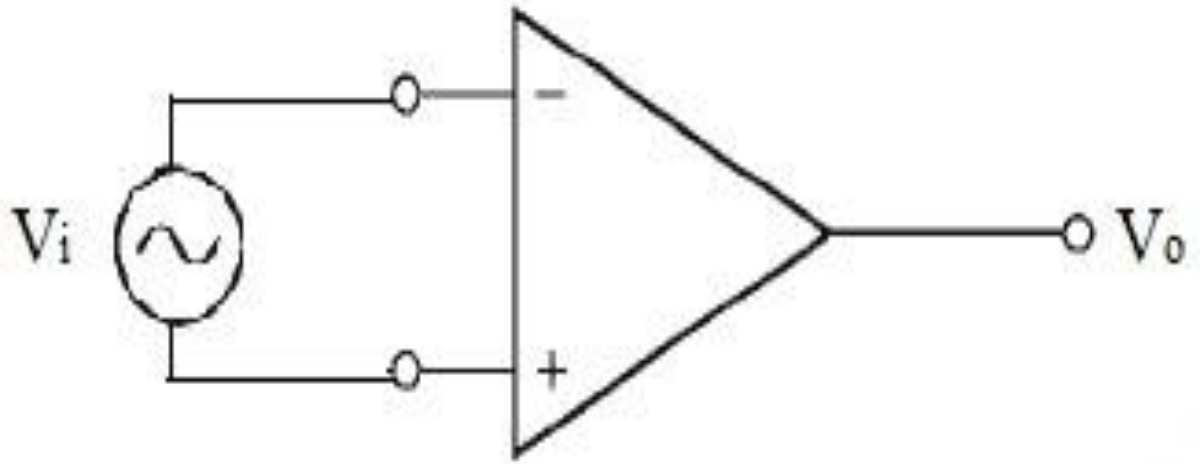


- Figure below shows the input is applied to Inverting terminal, connecting Non-inverting terminal to ground, which results in an output which is opposite in phase to the applied input signal.

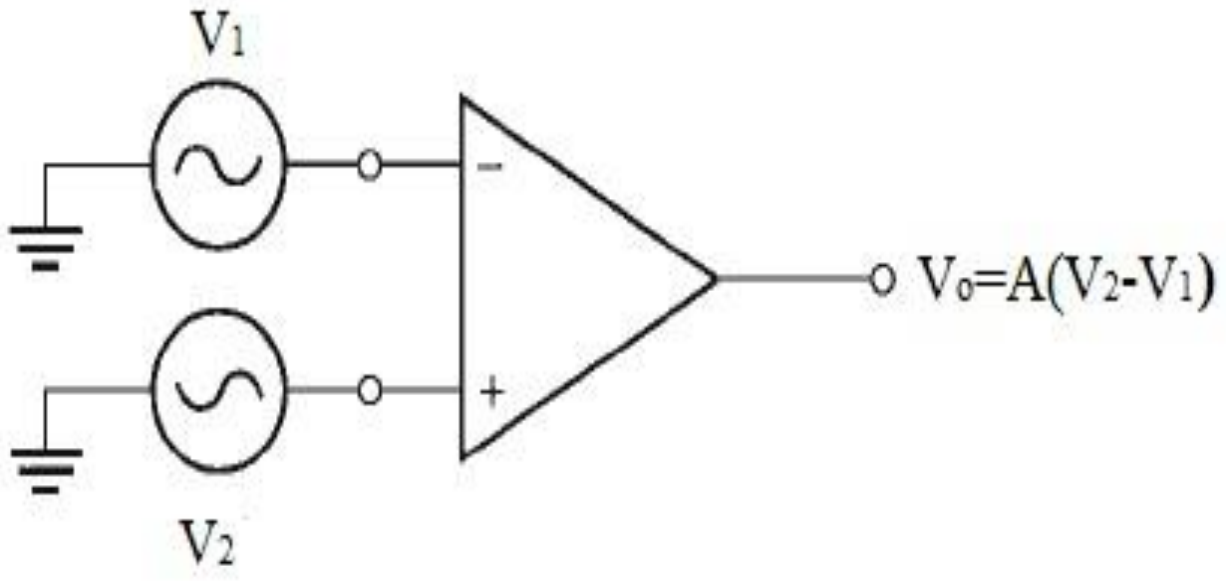


Double Ended Mode or differential Mode

- When the input is applied to both the input terminals it is called double ended operation or differential mode operation.
- Figure below shows an input V_i is applied between the two input terminals with the resulting amplified output in phase with the applied input between the non-inverting and inverting terminal.

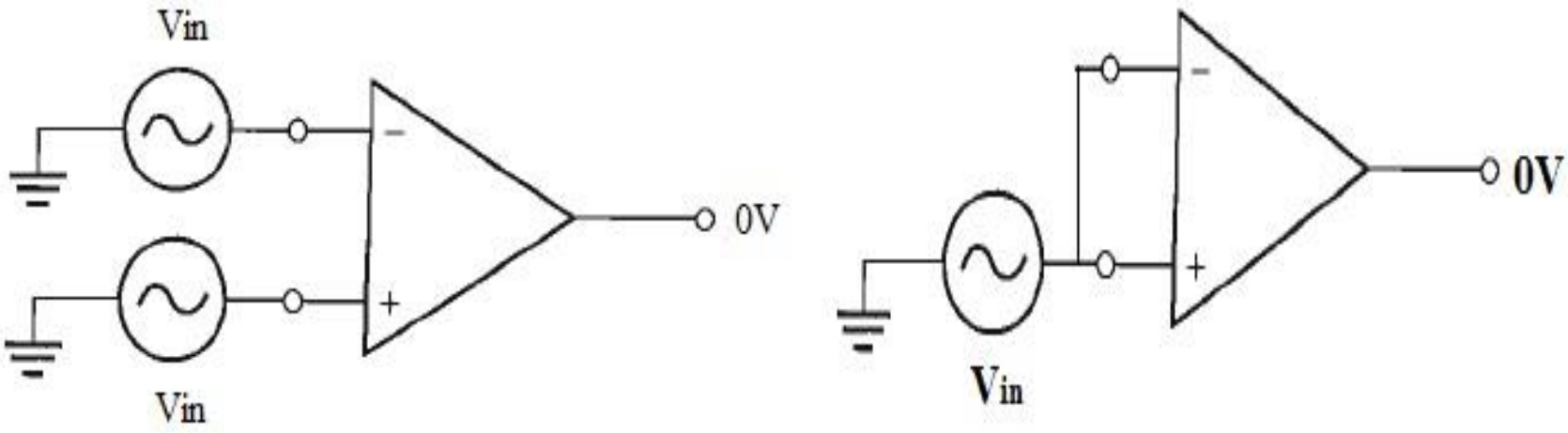


- Figure below shows two inputs V1 and V2 are applied to inverting and non-inverting terminals of an Op-amp which produces the output which is the difference signal (V2-V1) being amplified.



Common Mode operation or common Mode Rejection

- In common mode, two signal voltages of the same phase, frequency and amplitude are applied to the two inputs as shown in fig 4.
- When equal input signals are applied to both inputs, they cancel, resulting in a zero output voltage. This action is called common-mode rejection.
- But practically, a small output signal will result.
- The overall operation amplifies the difference signal while rejecting the common signal at the two inputs.



Op-amp parameters

1. Common Mode Rejection Ratio (CMRR)
2. Input Offset Voltage and Input Offset Current
3. Input bias current
4. Input Impedance
5. Output impedance
6. Slew rate

Op-amp parameters

1. Common Mode Rejection Ratio (CMRR):

- The measure of an amplifiers **ability to reject common-mode signal** is called Common-Mode Rejection Ratio.

- It can also be defined as the ratio of Differential gain (Ad) to the Common mode gain (Ac)

$$\text{CMRR} = \frac{A_d}{A_c}$$

- CMRR is often expressed in decibels (dB) as

$$\text{CMRR} = 20 \log \left(\frac{A_d}{A_c} \right)$$

- Higher the CMRR better is the performance of Op-amp.

2. Input Offset Voltage and Input Offset Current:

- The ideal Op-amp produces zero volts output for zero volts input.
- In a practical Op-amp, a small DC voltage appears at the output when no differential voltage is applied.
- The difference between the voltages present between the two input terminals when zero voltage is applied is called as **"Input offset Voltage, V_{OS}"**.

$$V_{os} = I_{os} R_{in}$$

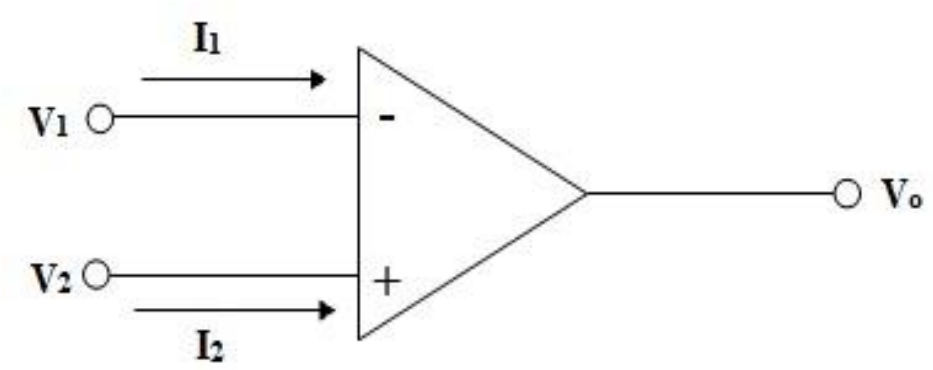
- In ideal op-amp, the two input bias currents are equal and thus their difference is zero.
- In a practical Op-amp the bias current is not exactly zero.
- The difference of the input bias currents is called as **"Input offset current, I_{OS}"**, expressed as an absolute value.

$$I_{os} = |I_1 - I_2|$$

3. Input bias current

- The input bias current is the **DC current required by the inputs of the amplifier** to properly operate the first stage.
- The input bias current is the average of both input currents and can be calculated as follows:

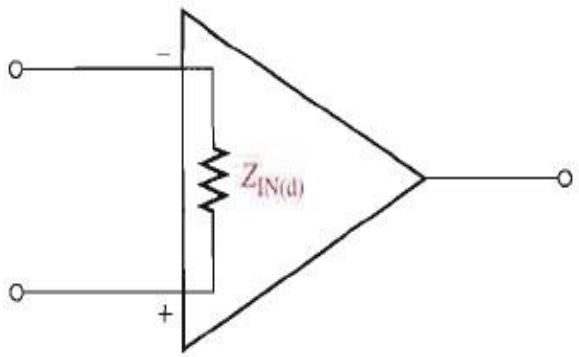
$$I_{Bias} = \frac{I_1 + I_2}{2}$$



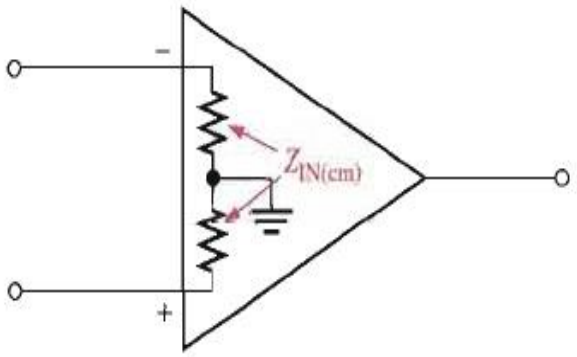
$$I_{Bias} = \frac{I_1 + I_2}{2}$$

4. Input Impedance

- Two basic ways of specifying the input impedance of an Op-amp are the **differential mode** and **common mode**.
- The differential input impedance is the total resistance between the inverting and the non-inverting inputs as shown in figure (a).
- Differential impedance is measured by determining the change in bias current for a given change in different input voltage.
- The common mode input impedance is the resistance between each input and ground as shown in figure (b).
- It is measured by determining the change in bias current for a given change in common-mode input voltage.



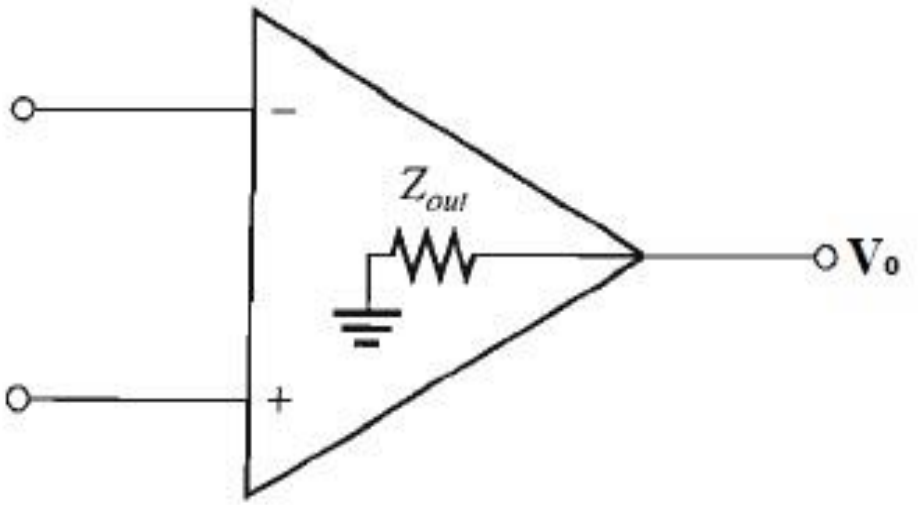
(a) Differential input impedance



(b) Common-mode input impedance

5. Output impedance

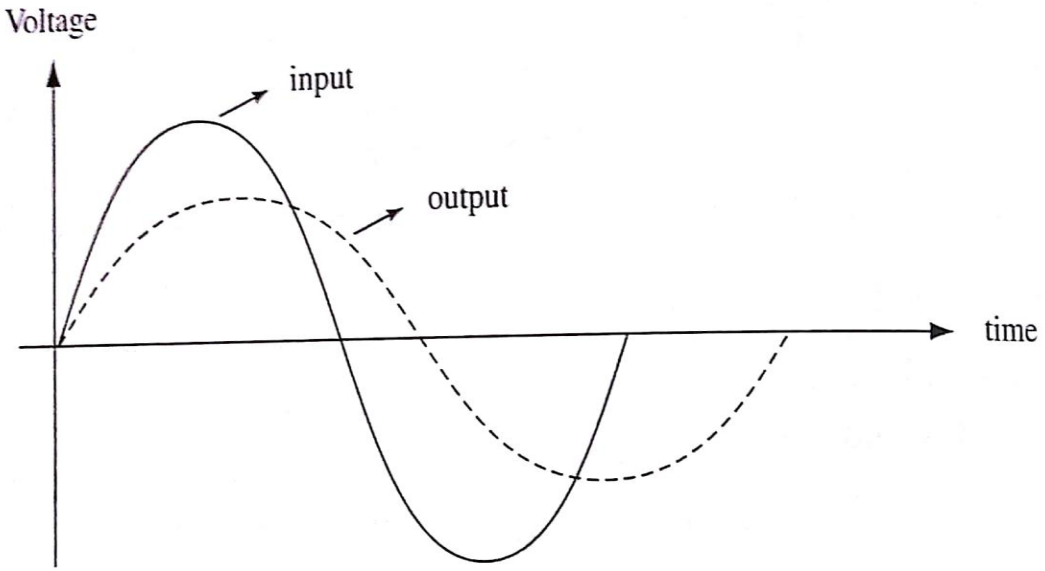
- Output impedance is the **resistance viewed from the output terminal** of the Op-amp, as shown in figure.



6. Slew rate

- Slew rate (SR) or Maximum Slew rate (MSR) is defined as the **maximum rate of change of output voltage with respect to time.**
- Slew rate can be expressed in Volts per microsecond.

$$\text{SR or MSR} = \frac{\Delta V_{out}}{\Delta t} \text{ V/}\mu\text{s}$$



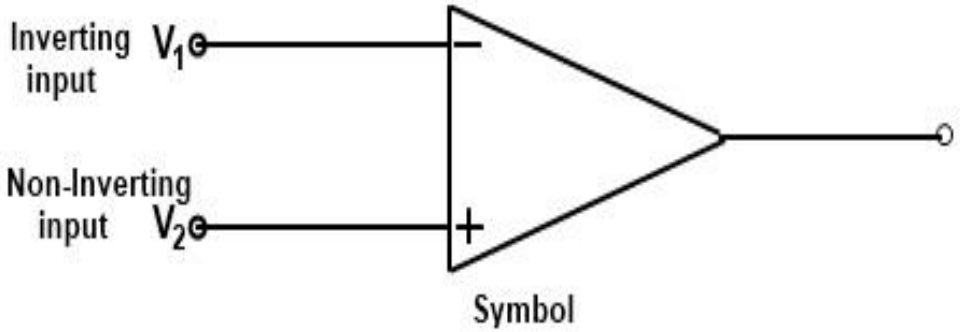
Characteristics of an ideal Op-amp

- **Infinite voltage gain (A= ∞):** The voltage gain of an ideal Op-amp is infinite.
- **Infinite input impedance ($R_i = Z_i = \infty$):** An ideal Op-amp does not draw any current from the voltage sources connected to its input terminal.
- **Zero output impedance ($R_o = 0$):** The output voltage of an ideal Op-amp is independent of the current drawn from it.
- **Infinite Bandwidth (BW= ∞):** An ideal Op-amp amplifies signals of any frequency with a constant gain.
- **Infinite CMRR (= ∞):** The common-mode rejection ratio of an ideal Op-amp is infinite.
- **Infinite Slew rate (SR= ∞):** The output voltage changes simultaneously with the input voltage.
- **PSRR=0:** The power supply rejection ratio is zero.
- The characteristics of an ideal Op-amp do not change with temperature.
- **Zero offset voltage:** The presence of small output voltage when $V_1=V_2=0$ is called an offset voltage.

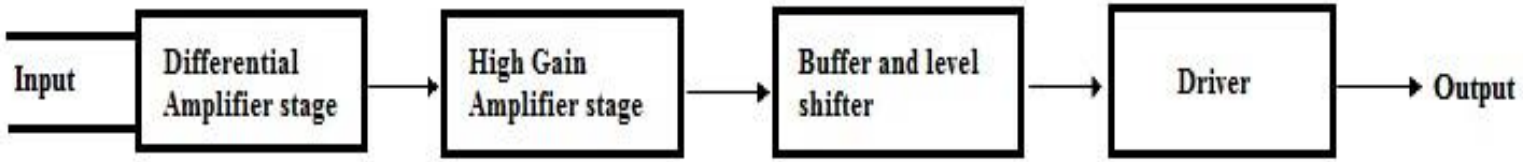
Block diagram of an Op-amp

- The symbol and Block diagram of an opamp is as shown in figure.

- It has different blocks namely, Differential amplifier, High Gain Amplifier, Buffer and Level shifter and the Driver.



Symbol



Block Diagram

1. Differential amplifier:

- It is the input stage of the Op-amp.
- It amplifies the difference of inputs i.e., (V_1-V_2)

2. High gain Amplifier:

- The output of differential amplifier stage is given as input to the High Gain Amplifier stage.
- This stage provides very high gain through a direct coupled amplifier.

3. Buffer and Level Shifter:

- The buffer is an emitter follower for matching the load.
- If the output is non-zero input, the level shifter makes it zero.

4. Driver:

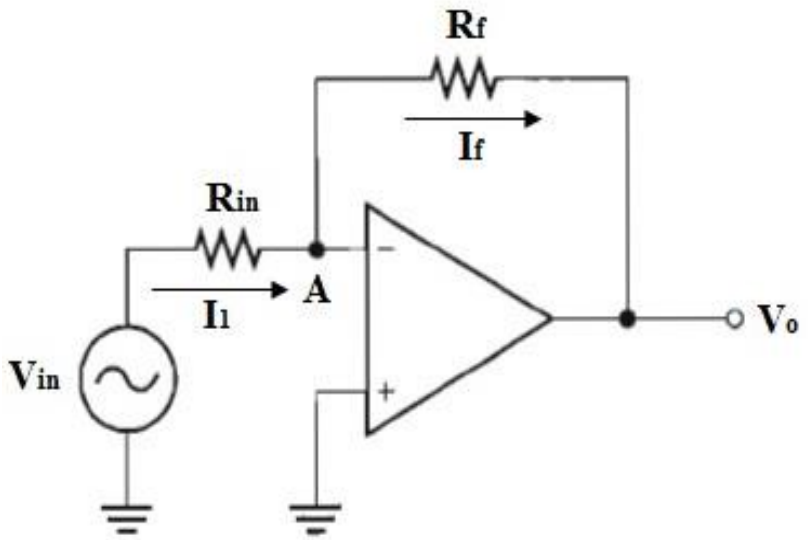
- It is a power amplifier used at the output stage.
- It produces very high amplified signals with respect to the input.

Applications of Op-amp

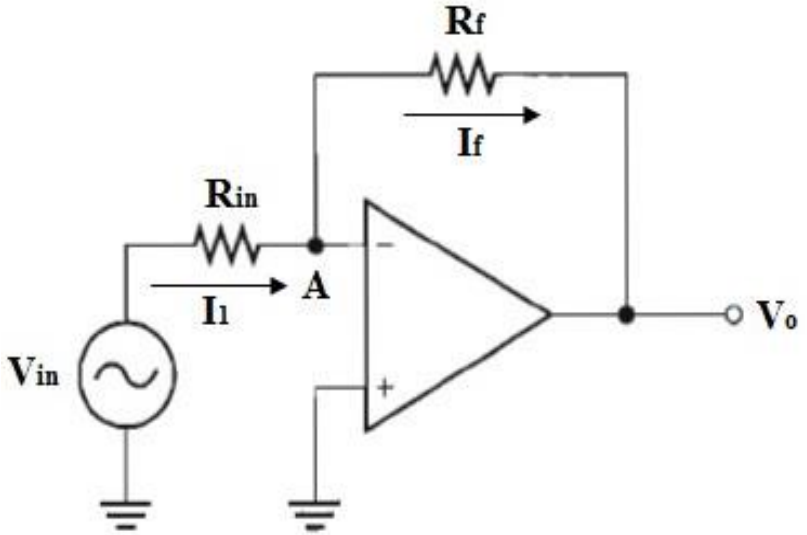
1. Inverting amplifier
2. Non-inverting amplifier
3. Adder or Summing Amplifier
4. Voltage follower
5. Integrator
6. Differentiator
7. Comparator

1. Inverting amplifier

- The Inverting amplifier circuit is as shown in figure
- The input is applied to the inverting terminal of the Op-amp and Non-inverting terminal is grounded.
- The potential at V_A will be zero because of virtual ground concept which states that both the input terminal will be at same potential.
- Also current to the input terminal of Op-amp is zero as $R_{in}=\infty$.



- The output is the amplified output which is negative to the input i.e., Inverted.
- The negative sign indicates that the polarity of the output is opposite to that of input, as shown in figure.



$$I_F = I_1$$

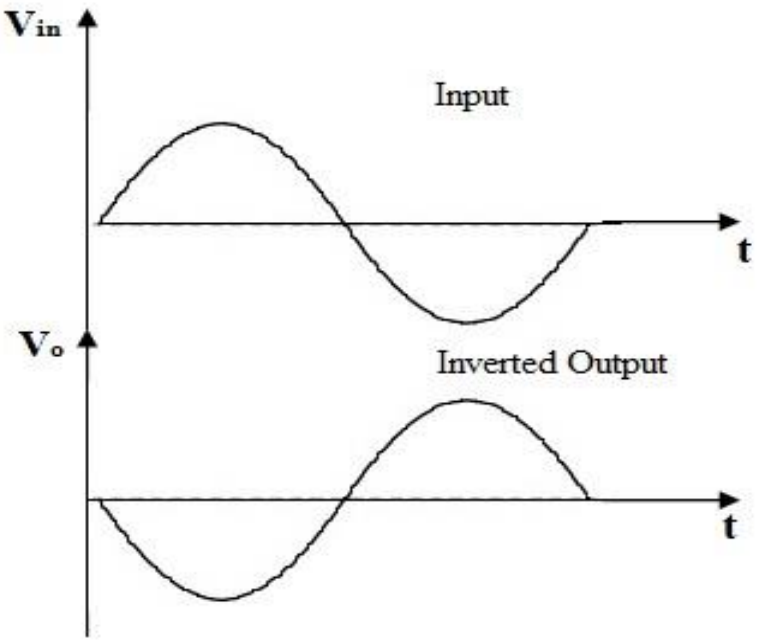
$$\frac{V_A - V_o}{R_F} = \frac{V_{in} - V_A}{R_{in}}$$

$$\frac{0 - V_o}{R_F} = \frac{V_{in}}{R_{in}}$$

$$\frac{-V_o}{R_F} = \frac{V_{in}}{R_{in}}$$

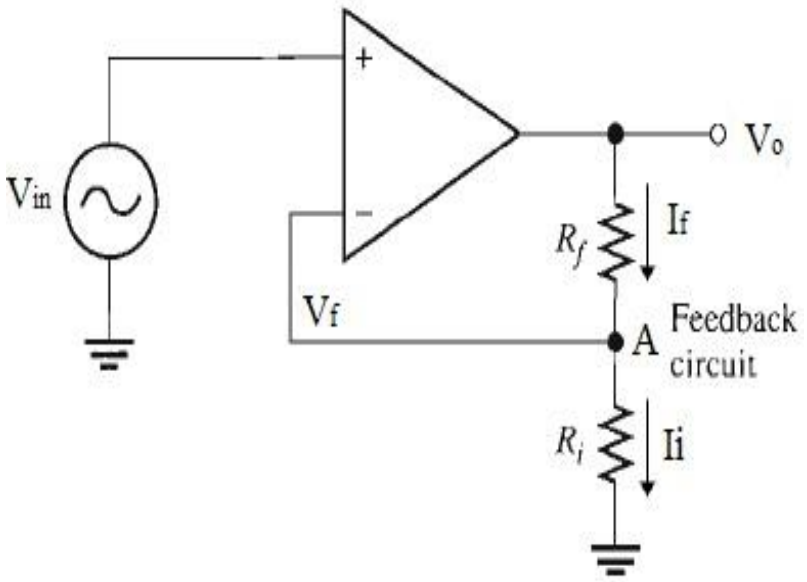
$$\frac{V_o}{V_{in}} = \frac{-R_F}{R_{in}}, \qquad A = \frac{-R_F}{R_{in}}$$

$$V_o = -\left(\frac{R_F}{R_{in}}\right) V_{in}$$



2. **Non-Inverting Amplifier**

- The Non-Inverting amplifier circuit is as shown in figure.
- Input is applied to the Non-Inverting terminal of the Op-amp and Inverting terminal is grounded.
- The potential at node A is equal to V_{in} because of virtual ground concept, i.e., $V_A = V_{in}$



- Applying KCL at node A,

$$I_F = I_i$$

$$\frac{V_o - V_A}{R_f} = \frac{V_A - 0}{R_i}$$

$$\frac{V_o}{R_f} = \frac{V_{in}}{R_i} + \frac{V_{in}}{R_f}$$

$$\frac{V_o}{R_f} = V_{in}\left(\frac{1}{R_i} + \frac{1}{R_f}\right)$$

$$\frac{V_o}{V_{in}} = R_f\left(\frac{1}{R_i} + \frac{1}{R_f}\right)$$

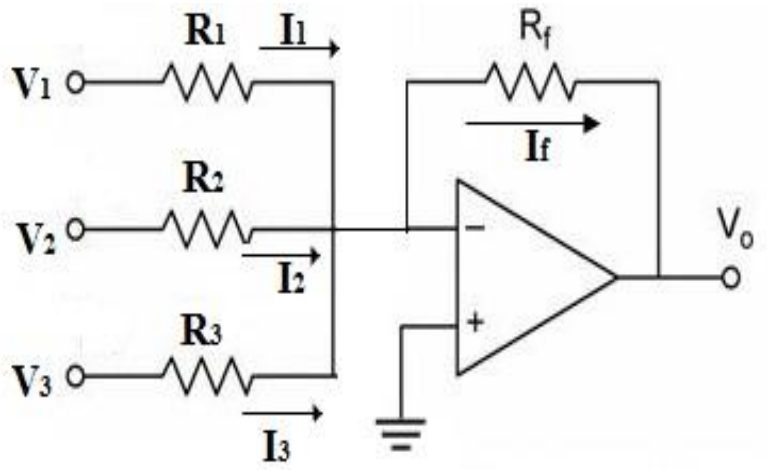
$$\frac{V_o}{V_{in}} = \left(\frac{R_f}{R_i} + \frac{R_f}{R_f}\right)$$

$$\frac{V_o}{V_{in}} = \left(\frac{R_f}{R_i} + 1\right), \qquad \frac{V_o}{V_{in}} = \left(1 + \frac{R_f}{R_i}\right) \qquad A = \left(1 + \frac{R_f}{R_i}\right),$$

- Output has the same sign of input. Hence it is in phase. Therefore, it is Non-inverting.

3. Summing Amplifier

- When more than one input is applied to either the inverting or to the non-inverting terminal, the output will be sum of all the voltages applied, each multiplied by a constant gain.
- Consider the Op-amp circuit shown in the figure 13 which has 3 inputs V_1, V_2 and V_3 given to the inverting terminal.



$$I_F = I_1 + I_2 + I_3$$

$$\frac{-V_o}{R_f} = \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}$$

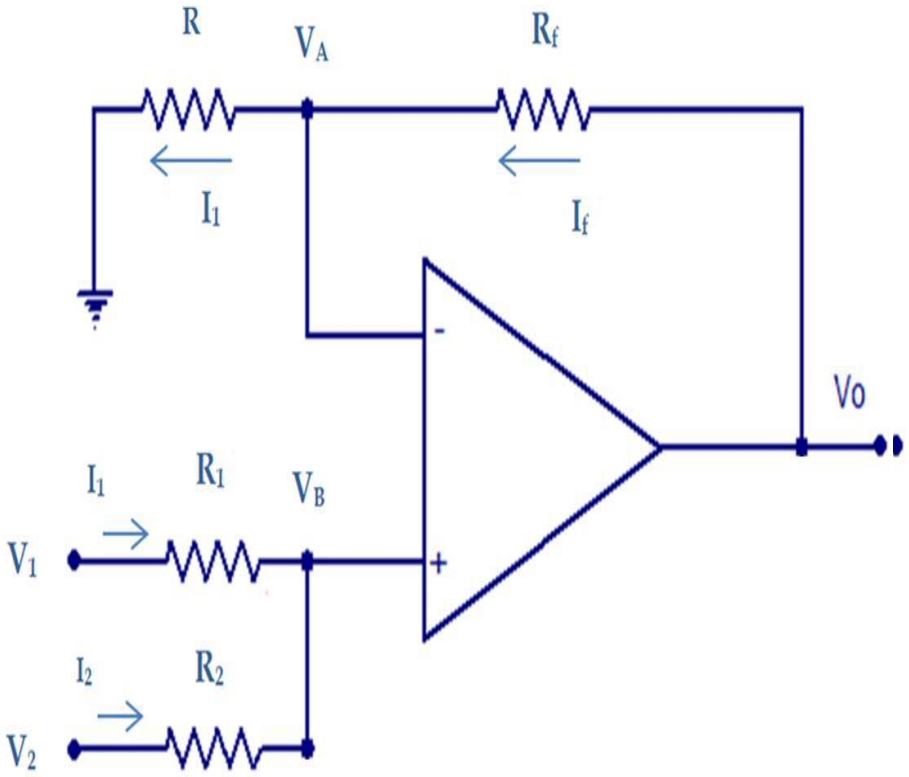
$$V_o = -\left\{R_f \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right)\right\}$$

$$V_o = -\left\{\left(\frac{R_f}{R_1}\right)V_1 + \left(\frac{R_f}{R_2}\right)V_2 + \left(\frac{R_f}{R_3}\right)V_3\right\}$$

If $R_1 = R_2 = R_3 = R_f$, $V_o = -(V_1 + V_2 + V_3)$

Summing Amplifier [Non-Inverting]

- When more than one input is applied to either the inverting or to the non-inverting terminal, the output will be sum of all the voltages applied, each multiplied by a constant gain.
- Consider the Op-amp circuit shown in the figure which has 2 inputs V_1 and V_2 given to the non-inverting terminal.
- Voltage at the node A, V_A is at the same potential of as of node B, V_B. $V_A = V_B$



- From the input side:

$$I_1 + I_2 = 0$$

$$But, I_1 = \frac{V_1 - V_B}{R_1} \; and \; I_2 = \frac{V_2 - V_B}{R_2}$$

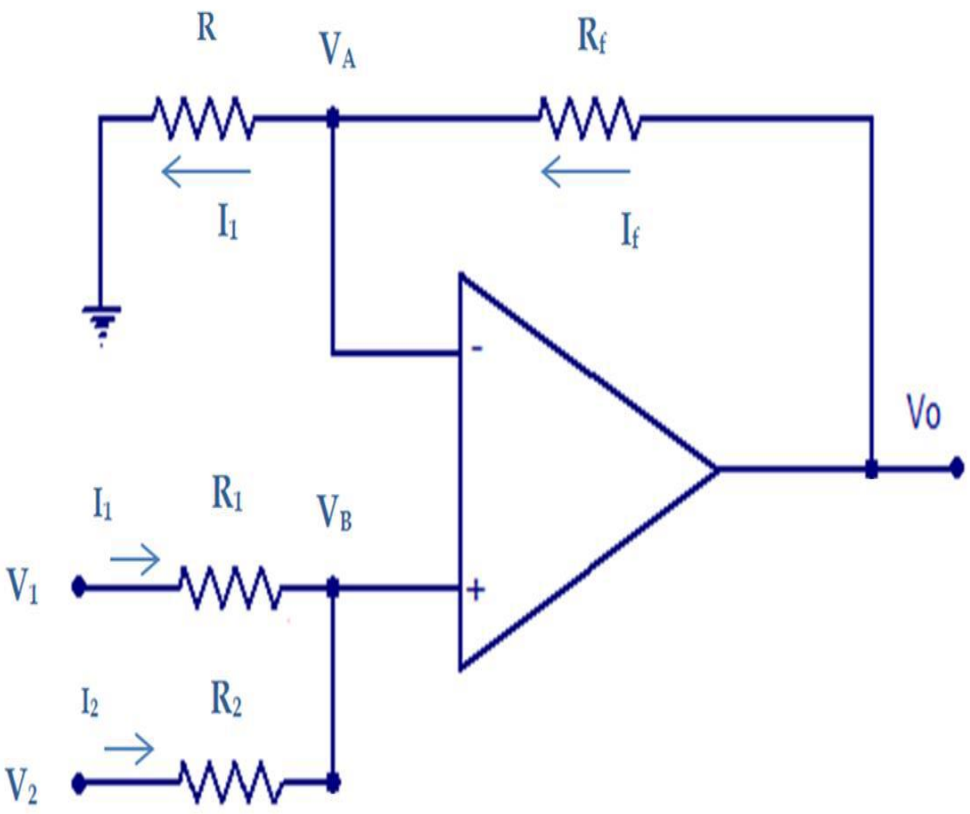
$$I_1 + I_2 = 0$$

$$\frac{V_1 - V_B}{R_1} + \frac{V_2 - V_B}{R_2} = 0$$

$$V_B = \frac{R_2 V_1 + R_1 V_2}{R_1 + R_2}$$

$$At \; node \; A, I_F = I_1$$

$$\frac{V_o - V_A}{R_f} = \frac{V_A - 0}{R}$$



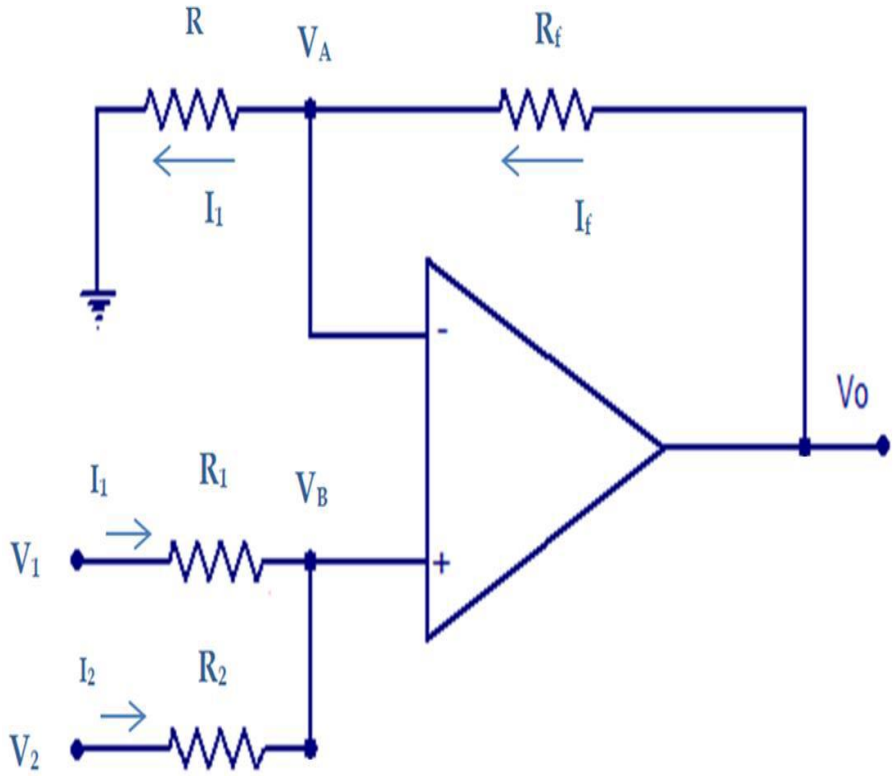
$$V_A = V_B \; (Due \; to \; Virtual \; ground)$$

$$\therefore V_A = 0 \; (\because V_B = 0)$$

$$\frac{V_o - V_B}{R_f} = \frac{V_B}{R}$$

$$\frac{V_o}{R_f} = \frac{V_B}{R_f} + \frac{V_B}{R} = V_B\left(\frac{R + R_f}{R}\right)$$

$$V_o = V_B\left(\frac{R + R_f}{R}\right)$$



$$V_o = \left(\frac{R_2V_1 + R_1V_2}{R_1 + R_2}\right)\left(\frac{R + R_f}{R}\right)$$

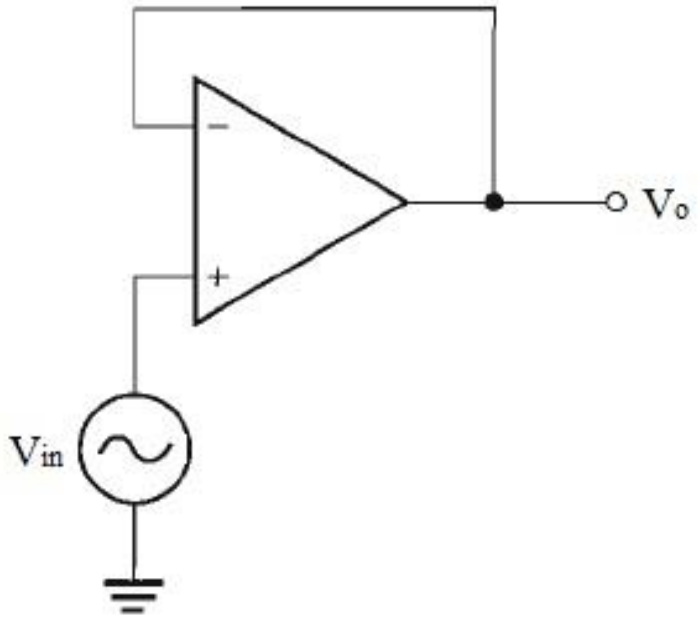
$$V_o = \left[\left(\frac{R_2(R + R_f)}{R(R_1 + R_2)} * V_1\right) + \left(\frac{R_1(R + R_f)}{R(R_1 + R_2)} * V_2\right)\right]$$

$$Assuming\ R_2 = R_1 = R_f = R$$

$$V_o = [V_1 + V_2]\ (Sum\ of\ two\ Inputs)$$

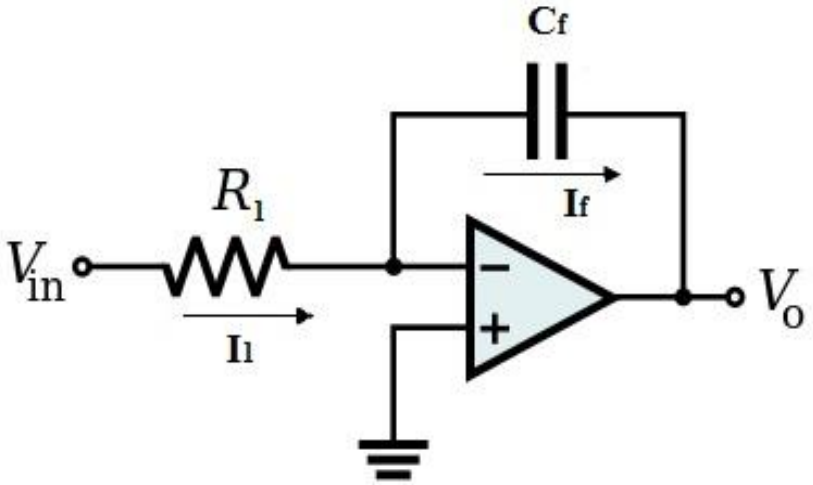
4. Unity follower or Voltage follower

- The voltage follower circuit is as shown in figure.
- It produces a unity gain with no polarity or phase reversal.
- The output will be equal to the input applied, i.e., $V_o=V_{in}$
- This circuit is called as voltage follower because the output will be same as input.



5. Integrator

- If the feedback component used is a capacitor, the resulting connection is called Integrator and the circuit can be written as shown in figure.
- Considering the voltage at the junction of R and X_c to be ground (since V_{in}), $I_F=I_1$.
- Capacitive impedance can be expressed as



$$X_C = \frac{1}{jWC_f} = \frac{1}{sC_f}, \quad \text{where } s = jw$$

$$I_1 = \frac{V_{in}}{R_1} \;\&\; I_F = \frac{-V_o}{X_c}, \quad I_F = I_1$$

$$\frac{-V_o}{X_c} = \frac{V_{in}}{R_1}$$

$$\frac{-V_o}{1/sC_f} = \frac{V_{in}}{R_1}$$

$$-sC_fV_o = \frac{V_{in}}{R_1}$$

$$\frac{V_o}{V_{in}} = -\frac{1}{R_1sC_f}$$

$$V_o = -\frac{1}{sR_1C_f}V_{in}$$

The above equation can be expressed in time domain as

$$V_o(t) = -\frac{1}{sR_1C_f}\int V_{in}(t)dt$$

6. Differentiator

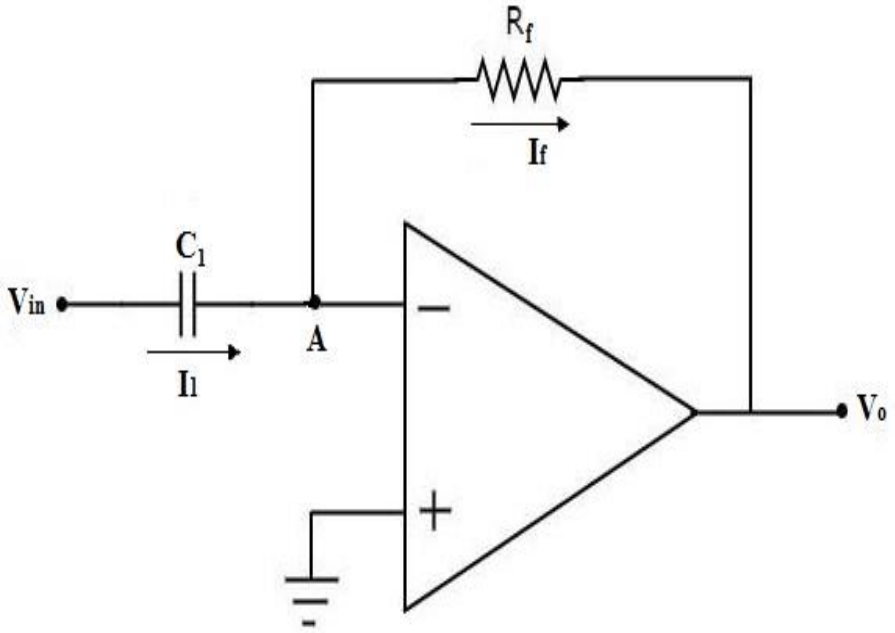
- In Differentiator circuit, the input is applied through capacitance C_1 as shown in the figure.

- Considering the voltage at node A is zero because of virtual ground concept.

$$I_F = I_1$$

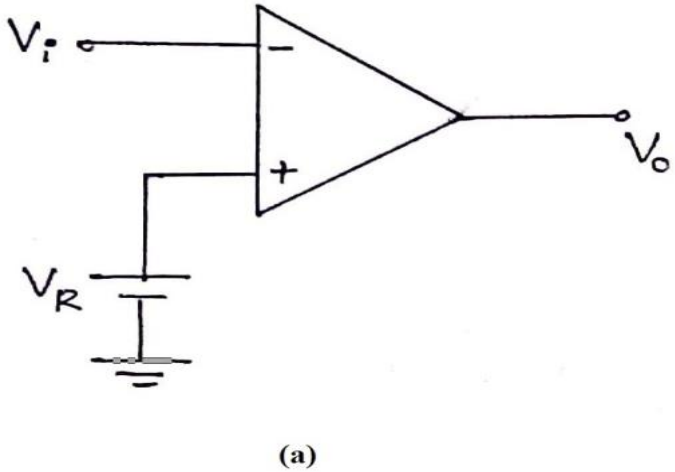
$$-\frac{V_o}{R_F} = C_1 \frac{dV_{in}}{dt}$$

$$V_o = -R_F C_1 \frac{dV_{in}}{dt}$$

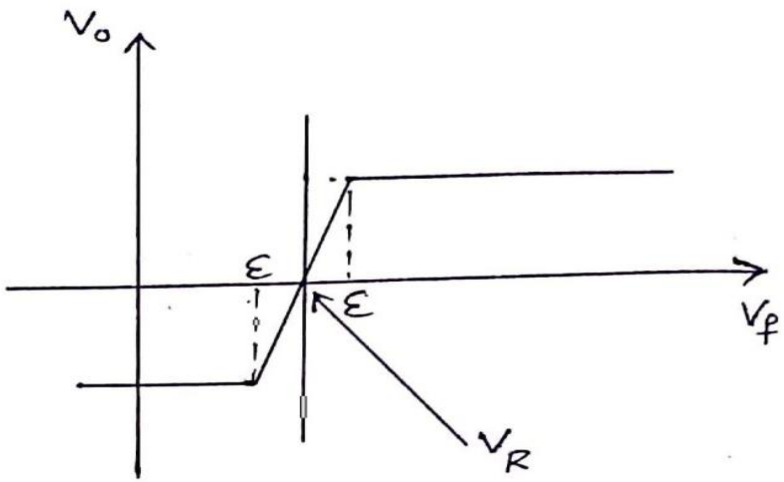


7. **Comparator**

- The Op-amp comparator circuit and the output are shown in figure (a) and (b).
- The saturation characteristic of an Op-amp in open loop is made use of in determining whether a signal is more or less than a certain reference value (V_R).
- If non-inverting terminal is grounded (V_R=0), the circuit becomes zero crossing detector.
- If V_i is sinusoidal, the output waveform will be rectangular assuming $\epsilon = 0$.



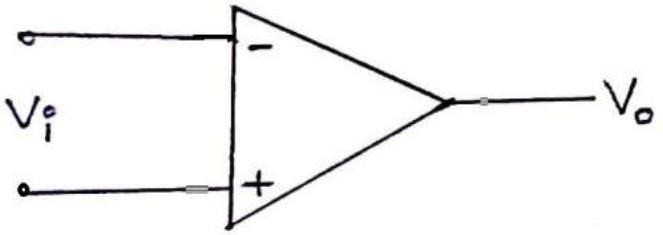
(a)



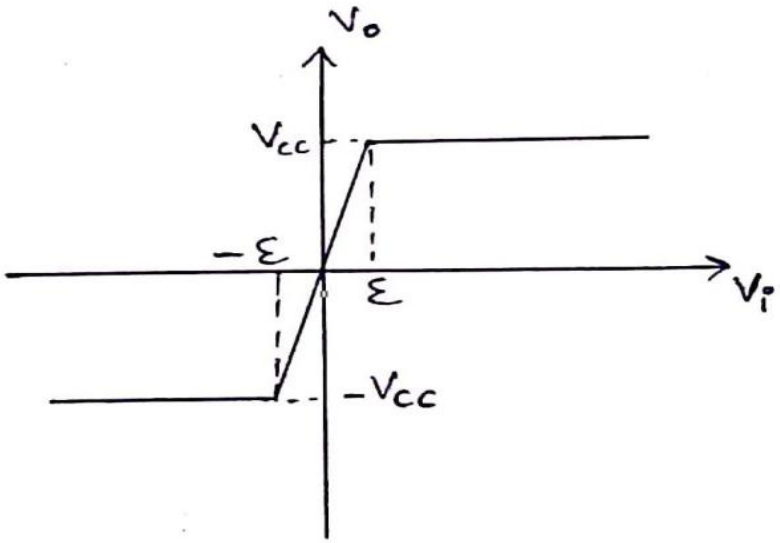
(b)

Transfer characteristics of Op-amp

- An Op-amp is a linear device with high gain.
- For small value of $V_i = \epsilon$, the output will be very high, i.e., V_{cc}.
- Beyond that the output gets saturated.
- Circuit diagram for open loop Op-amp and transfer characteristic is as shown in figures (a) and (b).



(a)



(b)


Thank You

MODULE 4

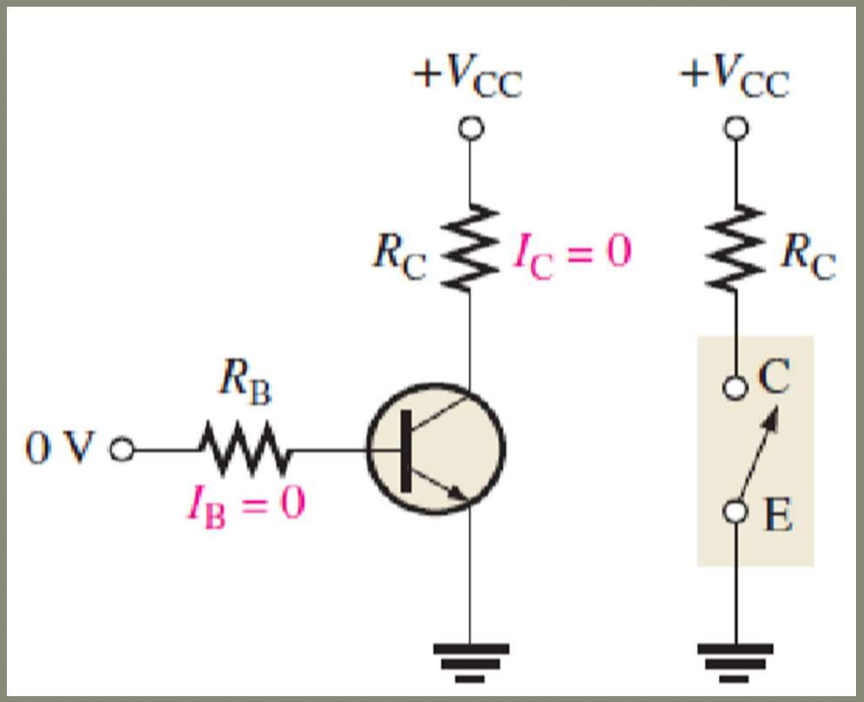
BJT Amplifier's & Oscillator's

Presented By:

GOUTHAM V
Asst. Prof. Dept. of ECE
BGSIT, B G Nagar

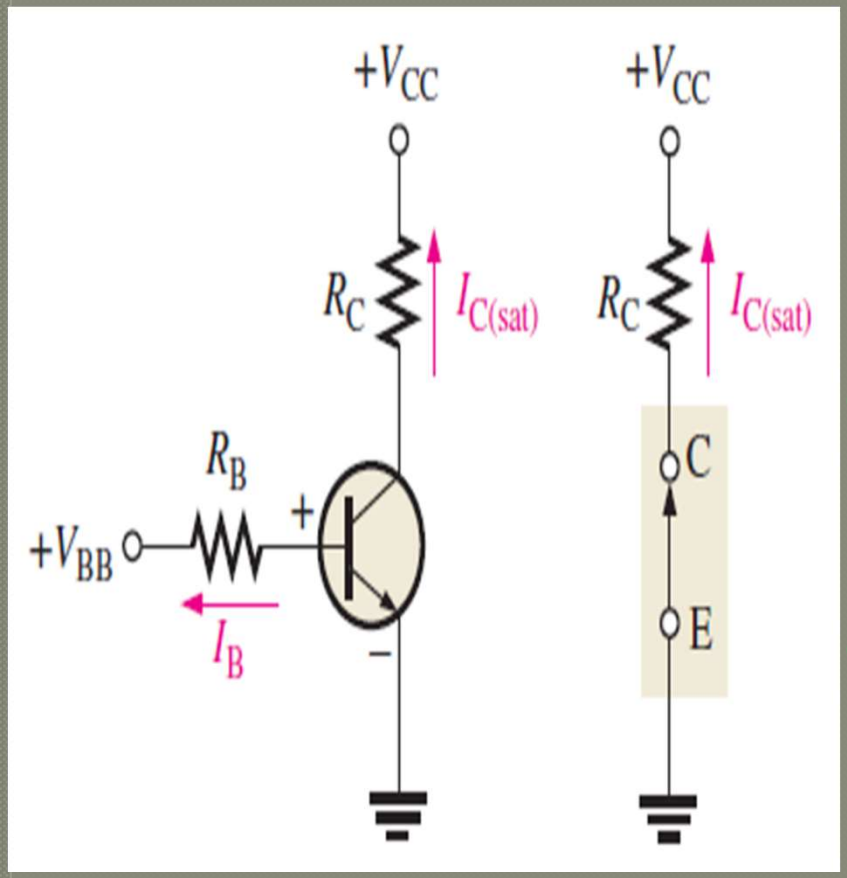
Switching Operation [Transistor as a Switch]:

- Figure below illustrates the basic operation of a BJT as a switching device.
- The device will be **ON** in the *Saturation Region* and will be **OFF** in the *Cut-off Region*.



- Considering the transistor in the cut-off region because the base-emitter junction is not forward-biased. In this condition, there is, ideally, an open between collector and emitter, as indicated by the switch equivalent.
- Neglecting leakage current, all of the currents are zero, and V_{CE} is equal to V_{CC}.

$$\mathbf{V_{CE(CUTOFF)} = V_{CC}}$$



- Considering the transistor in the saturation region, because the base emitter junction and the base-collector junction are forward-biased and the base current is made large enough to cause the collector current to reach its saturation value.
- In this condition, there is, ideally, a short between collector and emitter, as indicated by the switch equivalent.
- Actually, a small voltage drop across the transistor of up to a few tenths of a volt normally occurs, which is the saturation voltage, $V_{CE(sat)}$.

- The formula for collector saturation current is:

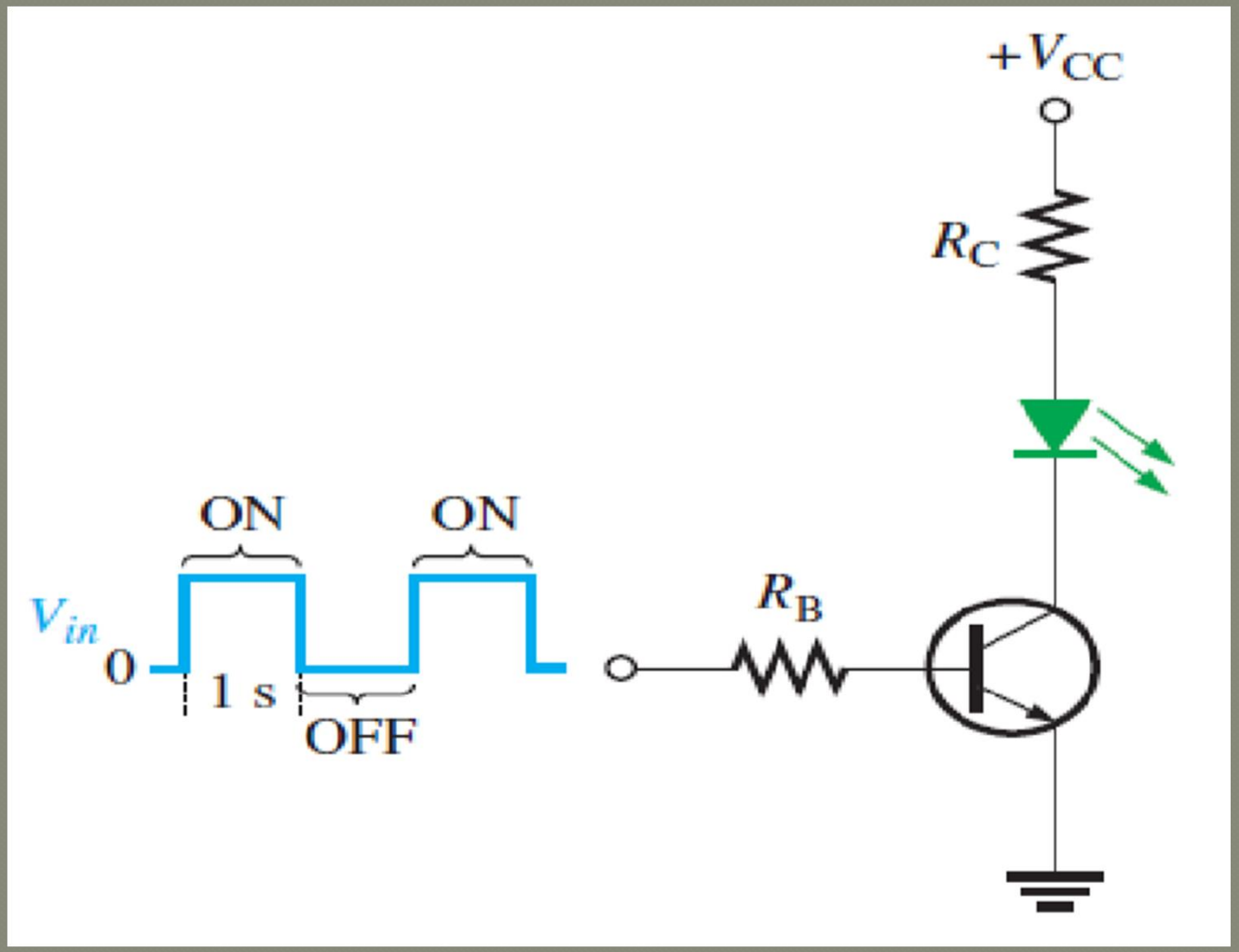
$$I_{C(sat)} = \frac{V_{CC} - V_{CE(sat)}}{R_C}$$

- Since $V_{CE(sat)}$ is very small compared to V_{CC}, it can be neglected.
- The minimum value of base current needed to produce saturation is

$$I_{B(min)} = \frac{I_{C(sat)}}{\beta_{DC}}$$

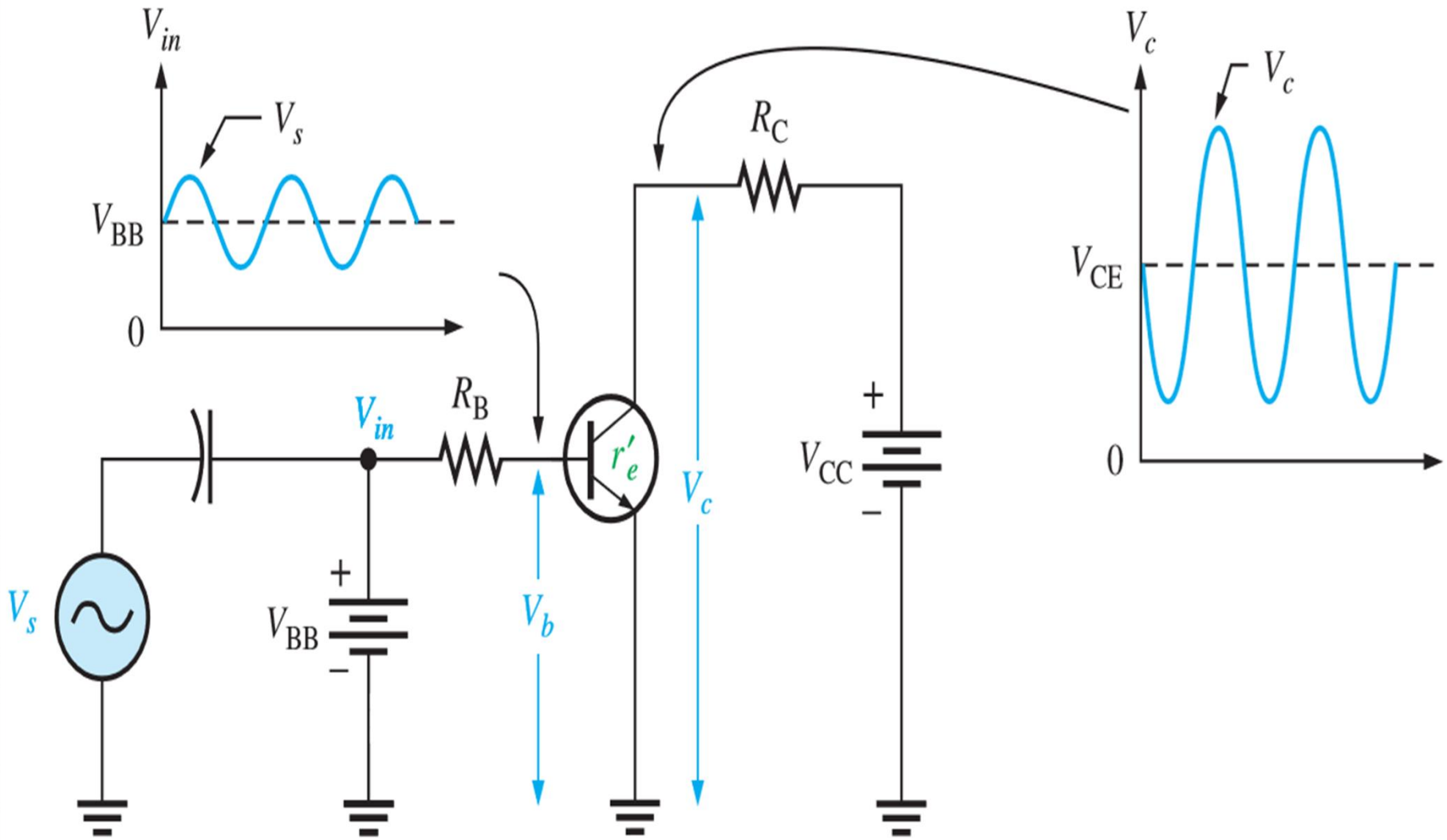
- Normally, I_B should be significantly greater than $I_{B(min)}$ to ensure that the transistor is saturated.

A Simple Application of a Transistor Switch to turn ON LED:



- The transistor in figure below is used as a switch to turn the LED on and off. For example, a square wave input voltage with a period of 2 s is applied to the input as indicated.
- When the square wave is at 0 V, the transistor is in cut-off; and since there is no collector current, the LED does not emit light.
- When the square wave goes to its high level, the transistor saturates. This, forward-biases the LED, and the resulting collector current through the LED cause it to emit light.
- Thus, the LED is on for 1 second and off for 1 second.

BJT as an Amplifier:



- BJT's in Active region is used as an Amplifier.
- **Transistor amplifies current, output current is gain times of controlling current i.e. $I_C = \beta * I_B$**
- The circuit connection of the BJT used as an amplifier is as shown.
- An AC voltage $\mathbf{V_S}$ is applied with the DC bias voltage $\mathbf{V_{BB}}$ by capacitor coupling to the Base of the transistor through base resistor $\mathbf{R_B}$.
- DC bias voltage $\mathbf{V_{CC}}$ is applied to the collector through collector resistor $\mathbf{R_C}$.

- Thus I_C produces AC voltage across R_C which produces an amplified and inverted output as shown in the figure.
- The AC base voltage V_B is given by:

$$V_B = I_E * r'_E$$

- The AC collector voltage V_C across R_C is given by:

$$V_C = I_C * R_C$$

- Since $I_C \cong I_E$
- V_B is an input voltage given by $V_B = V_S - I_B * R_B$.
- V_C is an output voltage.
- Voltage gain A_V is defined by:

$$A_V = \frac{V_C}{V_B} = \frac{I_C * R_C}{I_E * r'_e} \cong \frac{I_E * R_C}{I_E * r`_E}$$

$$A_V \cong \frac{R_C}{r`_E}$$

- Thus the above equation shows that the transistor provides amplification in the form of voltage gain.

Feedback Circuits:

- *The feedback-amplifier can be defined as an amplifier which has feedback line that exists between output to input.*
- *In amplifier, feedback is the limitation which calculates the sum of feedback given in the amplifier.*
- *Feedback is mainly used to reduce the noise as well as to make the operation of an amplifier is constant.*
- *Feedback amplifier can be classified into two types based on the feedback signal, such as positive & negative feedback amplifier.*

Positive Feedback Amplifier:

- The positive feedback can be defined as when the feedback current or voltage is applied for increasing the input voltage.
- Direct feedback is another name of this positive feedback. Because positive feedback generates unnecessary distortion; it is not often used in amplifiers. But, it amplifies the original signal power and can be used in oscillator circuits.

Negative Feedback Amplifier:

- The negative feedback can be defined as if the feedback current or voltage can be applied for reducing the amplifier input, then it is called as negative feedback.
- Inverse feedback is another name of this negative feedback. This kind of feedback is regularly used in amplifier circuits.

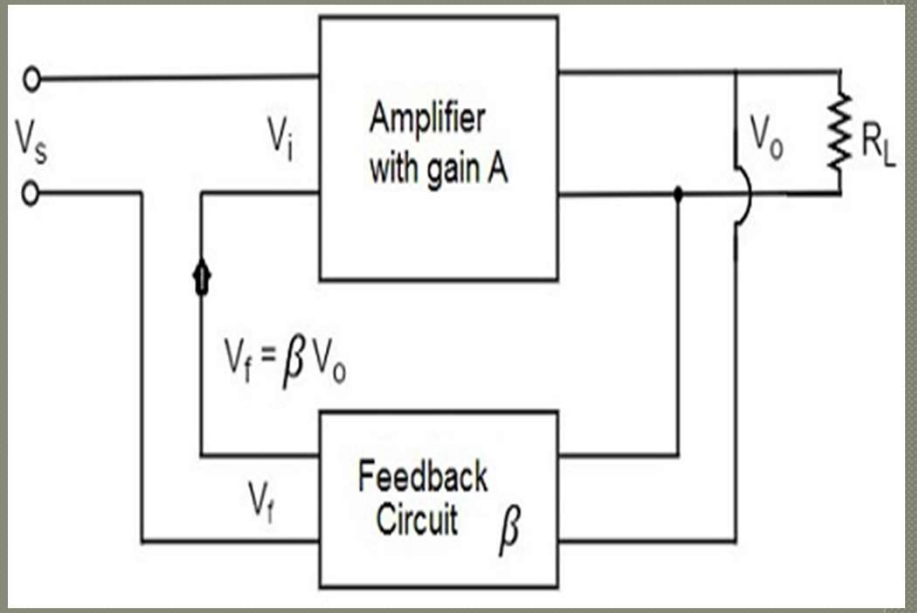
- There are *four basic amplifier topologies* for connecting the feedback signal. Both the current as well as voltage can be feedback toward the input in series otherwise in parallel.

1. ***Voltage Series feedback amplifier***
2. ***Voltage Shunt feedback amplifier***
3. ***Current Series feedback amplifier***
4. ***Current Shunt feedback amplifier***

Voltage Series Feedback Amplifier

- In this type of circuit, a portion of the o/p voltage can be applied to the input voltage in series through the feedback circuit.

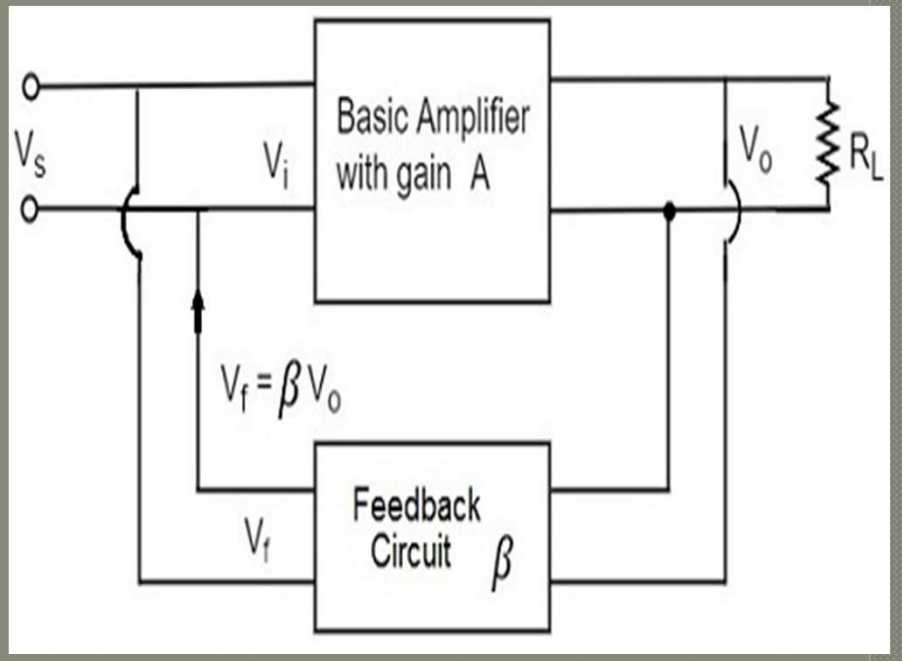
- The block diagram of the voltage series feedback-amplifier is shown below, by which it is apparent that the feedback circuit is located in shunt by means of the output although in series by means of the input.



- When the feedback circuit is allied in shunt through the output, then the ***output impedance*** will be ***reduced*** and the ***input impedance*** is ***increased*** because of the series connection with the input.

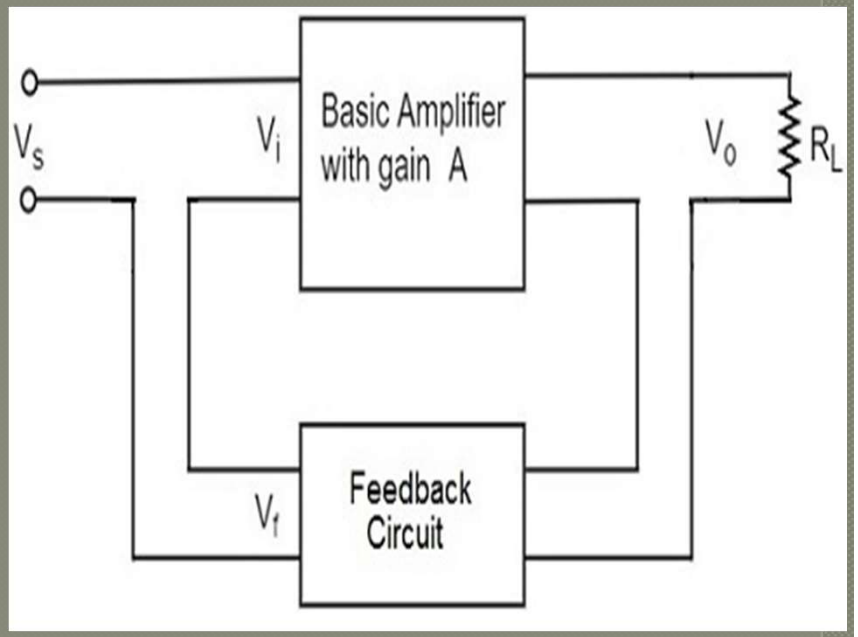
Voltage Shunt Feedback Amplifier

- In this type of circuit, a portion of the output voltage can be applied to the input voltage in parallel with through the feedback circuit.
- The block diagram of the voltage shunt feedback-amplifier is shown below, by which it is apparent that the feedback circuit is located in shunt by means of the output as well as the input.
- When the feedback circuit is allied in shunt through the output as well as the input, then both the ***output impedance & the input impedance will be decreased***.



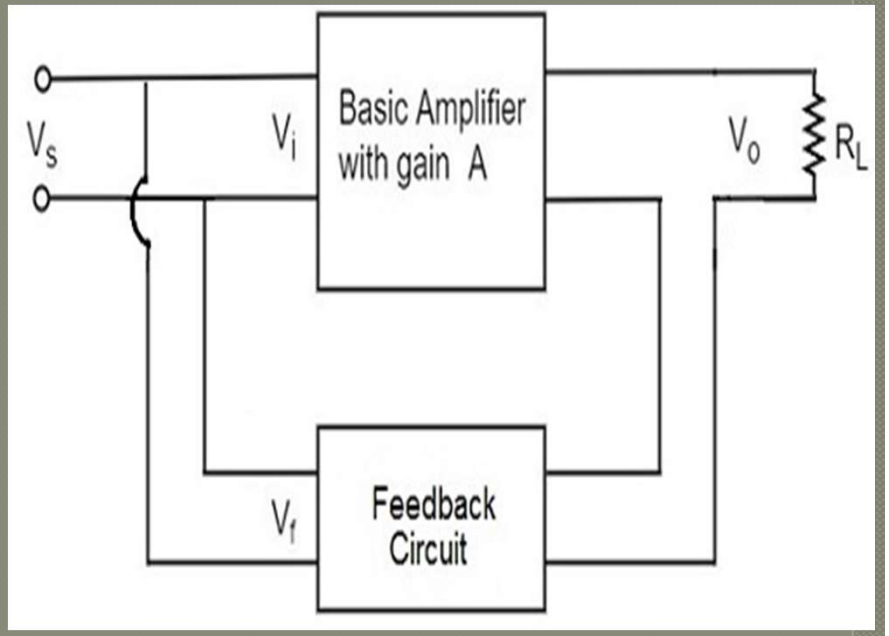
Current Series Feedback Amplifier

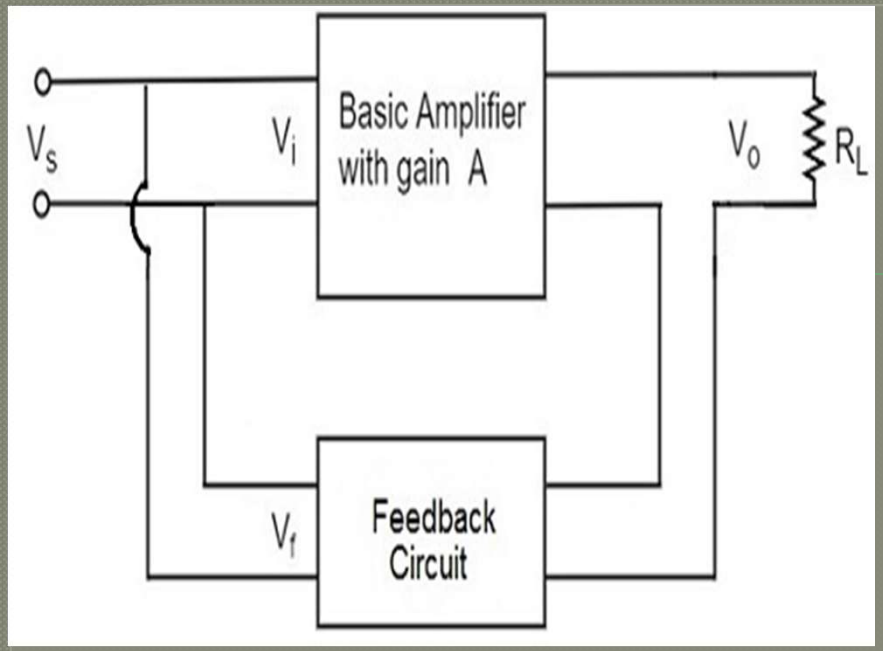
- In this type of circuit, a portion of the o/p voltage is applied to the input voltage in series through the feedback circuit.
- The block diagram of the current series feedback-amplifier is shown below, by which it is apparent that the feedback circuit is located in series by means of the output as well as the input.
- When the feedback circuit is allied in series through the output as well as the input, ***then both the output impedance & the input impedance will be increased***.

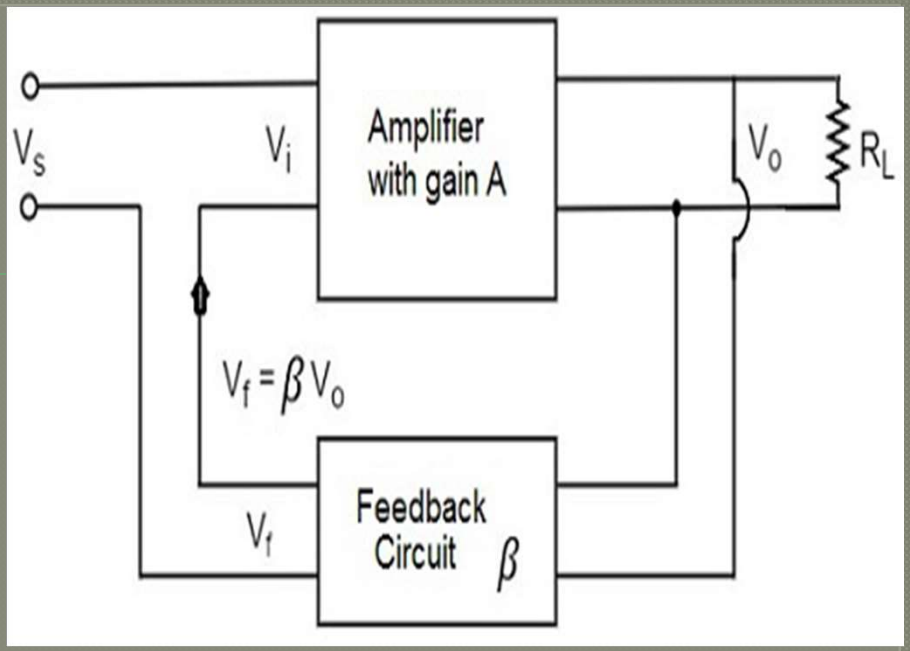


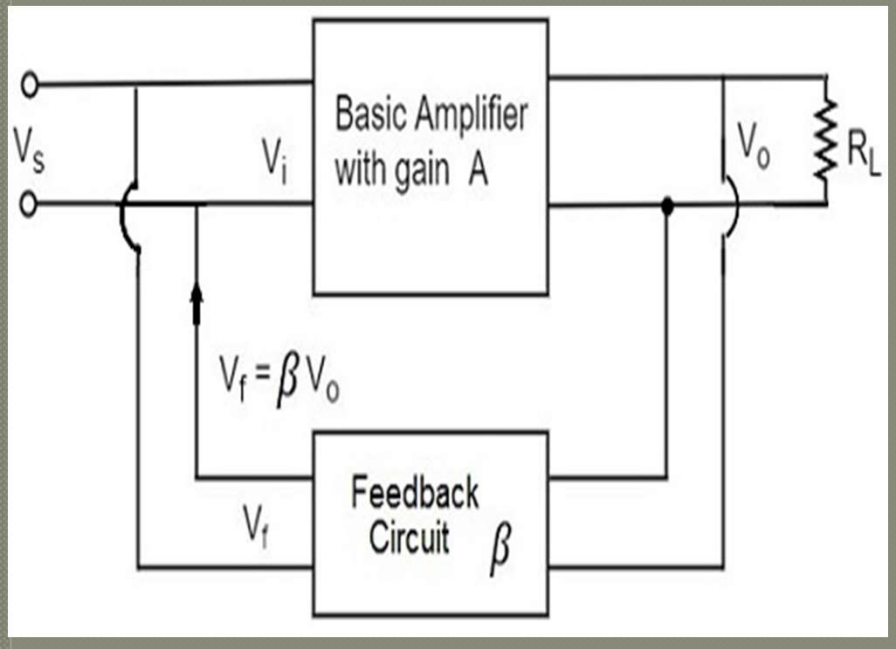
Current Shunt Feedback Amplifier

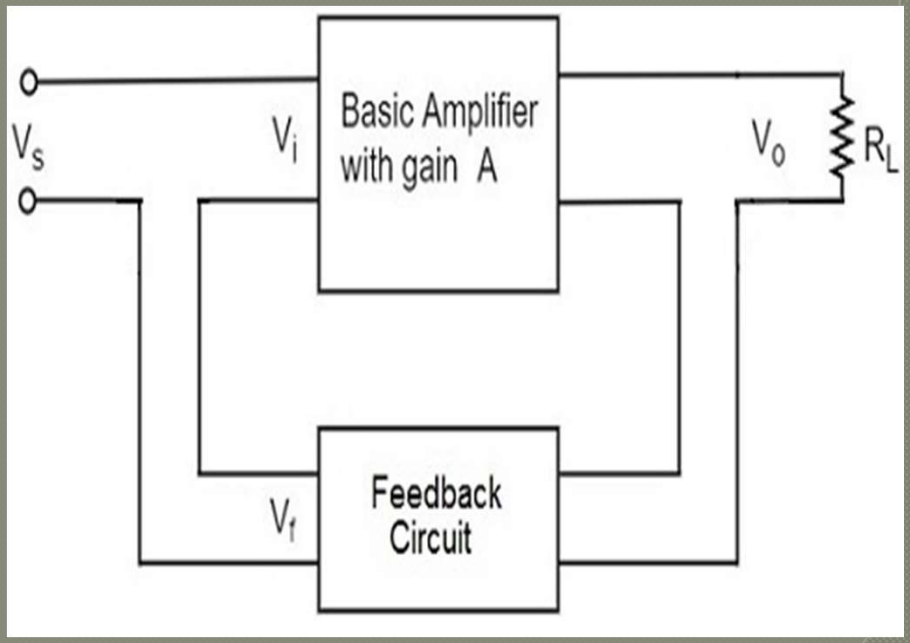
- In this type of circuit, a portion of the o/p voltage is applied to the input voltage in shunt through the feedback circuit.
- The block diagram of the current shunt feedback-amplifier is shown below, by which it is apparent that the feedback circuit is located in shunt by means of the output as well as the input.
- When the feedback circuit is allied in series through the o/p however in parallel with the input, then the ***output impedance will be increased*** & because of the parallel connection with the input, the ***input impedance*** will be ***decreased***.




Basic Amplifier
with gain A
V_s
V_i
V_o
R_L
V_f
Feedback
Circuit

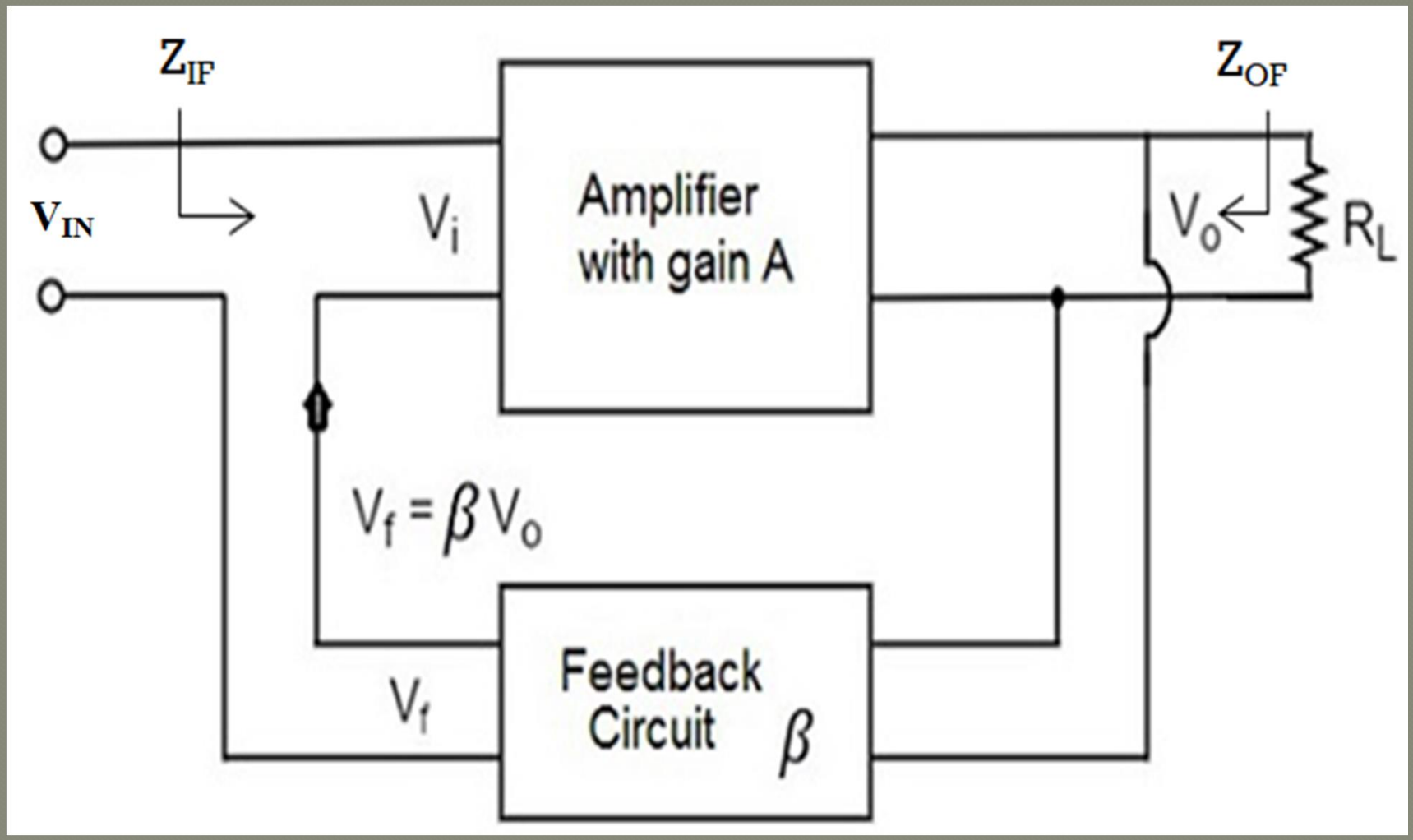

Amplifier
with gain A
V_s
V_i
V_o
R_L
$V_f = \beta V_o$
V_f
Feedback
Circuit β


Basic Amplifier
with gain A
V_s
V_i
V_o
R_L
$V_f = \beta V_o$
V_f
Feedback
Circuit β


Basic Amplifier
with gain A
V_s
V_i
V_o
R_L
V_f
Feedback
Circuit

Voltage Series:

- Considering the voltage series feedback which is called as Series-Parallel feedback is shown in the below figure. Here the feedback is negative.



- From the figure,

$$V_i = V_{in} - \beta V_o$$

$$V_o = AV_i = A\,(V_{in} - \beta V_o) = A*V_{in} - A*\beta*V_o$$

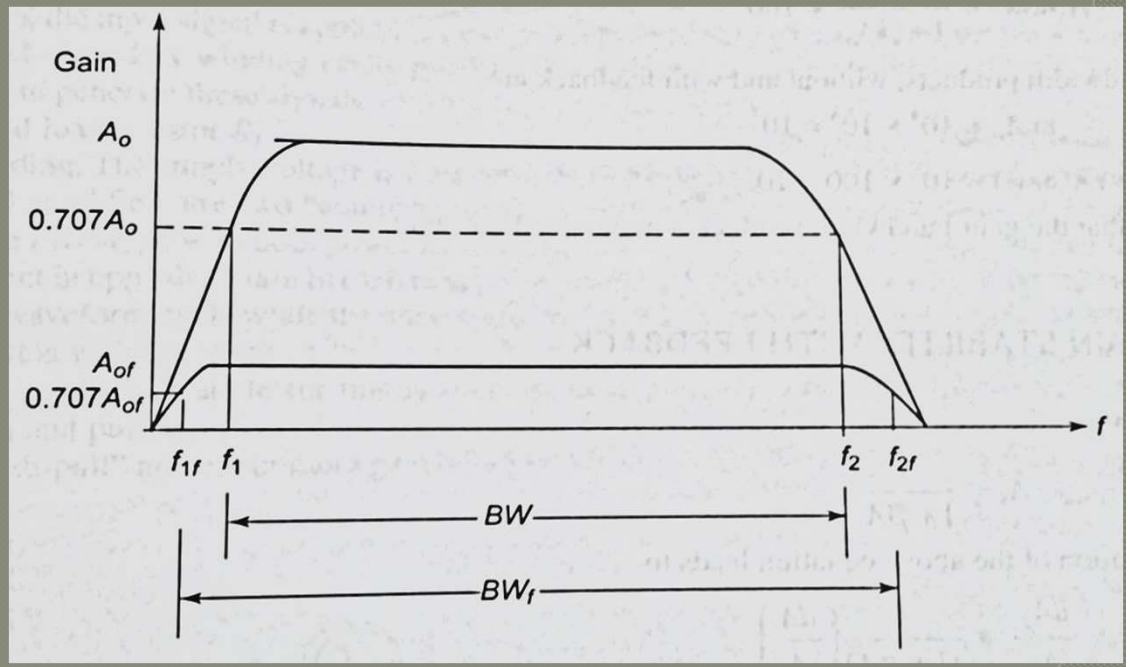
- Gain with feedback equation is as follows which is applicable to all types of feedback circuits.

$$\frac{V_o}{V_{in}} = A_F = \frac{A}{1+\beta A}$$

- The amplifier gain reduces by a factor of $(1 + \beta A)$.
- Input impedance with feedback, $Z_{if} = Z_i\ (1 + \beta A)$ increases and output impedance with feedback, $Z_{of} = Z_o/(1 + \beta A)$ decreases.
- If $\beta A \gg 1$ then A_F is given by $A_F = \frac{1}{\beta}$
- From the above equation we can conclude that feedback gain is independent of amplifier gain A.
- Any variation in magnitude of A does not appear in A_F, which means A_F has high gain stability.

Gain and Bandwidth of Feedback Amplifier:

- We know that negative feedback reduces the amplifier gain, and hence it increase its bandwidth.
- In RC – coupled amplifiers, the gain reduces at low frequency and high frequency ends. So βA_o is no longer much more than unity.
- As a result, the percent reduction in gain is less at the two frequency ends compared to the mid-band.
- The reduction in gain and increases in bandwidth of feedback amplifier is as shown below:



- As $f_1 \ll f_2$ and $f_{1f} \ll f_{2f}$ therefore,

$$BW \approx f_2;$$

$$BW_f \approx f_{2f}$$

- It can be shown that, $A_o f_2 = A_o f_{2f}$

Constant product of gain bandwidth.

Gain Stability with feedback:

- Overall gain with negative feedback is $\boldsymbol{A_F = \frac{A}{1+\beta A}}$

- Differentiation of above equation gives:

$$\frac{dA_f}{A_f} = \frac{1}{1+\beta A}\left(\frac{dA}{A}\right);$$

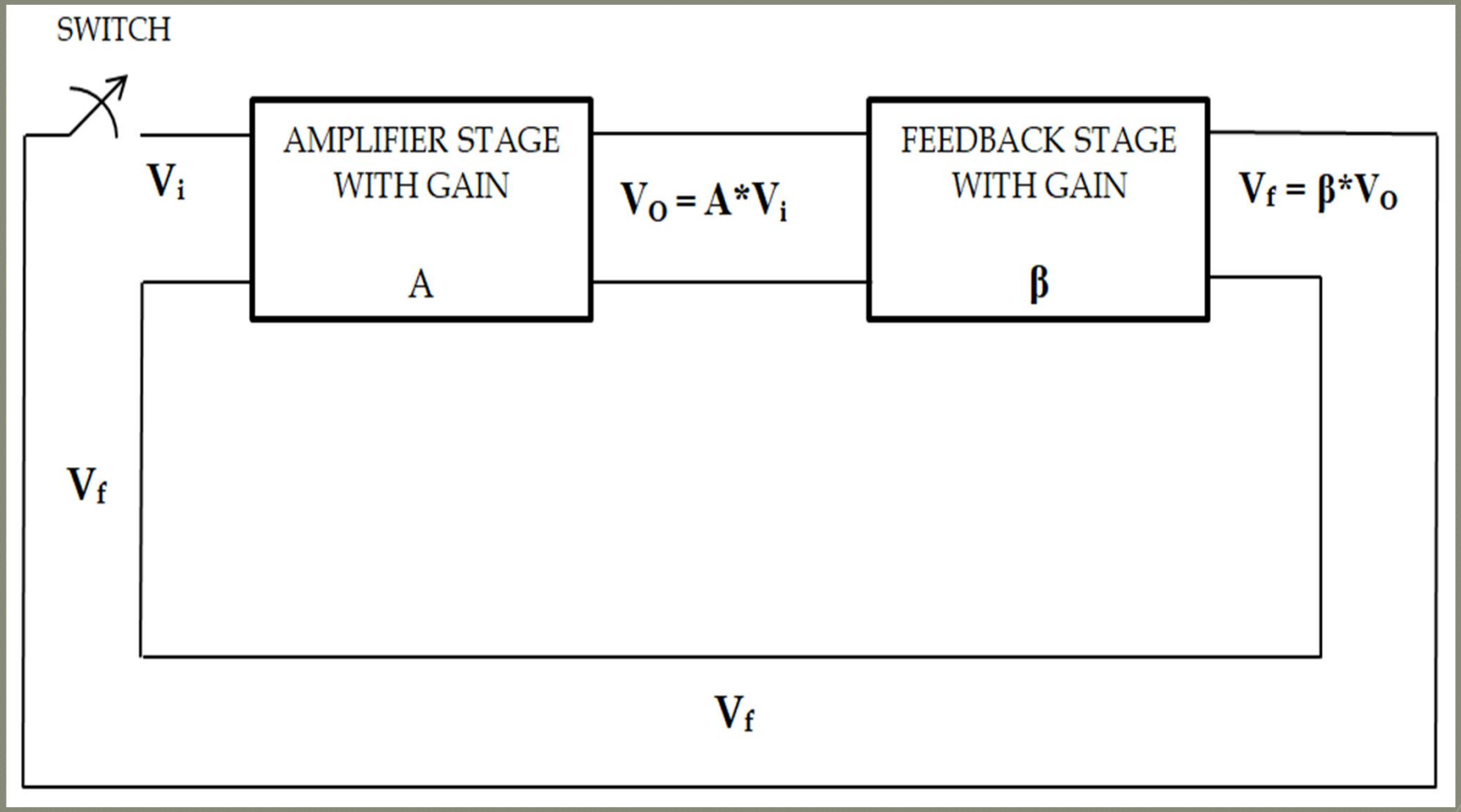
$$\frac{dA_f}{A_f} = \frac{1}{\beta A}\left(\frac{dA}{A}\right) = \text{for } \beta A \gg 1$$

- This shows that a relative change (dA/A) in the basic amplifier gain is reduced by the factor of βA in the relative change (dA_f/A_f) in the overall gain of the feedback amplifier.

Oscillator Operation and Barkhausen Criterion:

- The use of positive feedback that results in a feedback amplifier having closed loop gain $|A_f|$ greater than Unity (1) and satisfies the phase condition will result in operation as an Oscillator circuit.
- An oscillator circuit generates oscillations with the feedback circuit, without any input which will be of constant amplitude and frequency.
- If the output signal varies sinusoidal with time, the circuit id referred to as a "Sinusoidal Oscillator".
- If the output voltage rises quickly to one voltage level and later drops quickly to another voltage level, the circuit is generally referred to as "Pulse or Square Wave Oscillator".

Barkhausen Criterion:



- Consider a basic inverting amplifier with an gain **A** and the feedback netwrok gain **β**.

- The input V_i is applied to the Amplifier through a switch whose output is V_O which is 180^o phase shifted output. This will be fed as input to the feedback stage whose output is V_f .

- When the switch is closed, the input V_i is applied to the amplifier.

$$V_O = A*V_i$$

- For an oscillator, the output of the feedback circuit should drive the amplifier stage, so V_f should be equal to V_i. Hence for V_f to be inphase with V_i feedback circuit should produce 180^o phase shift.

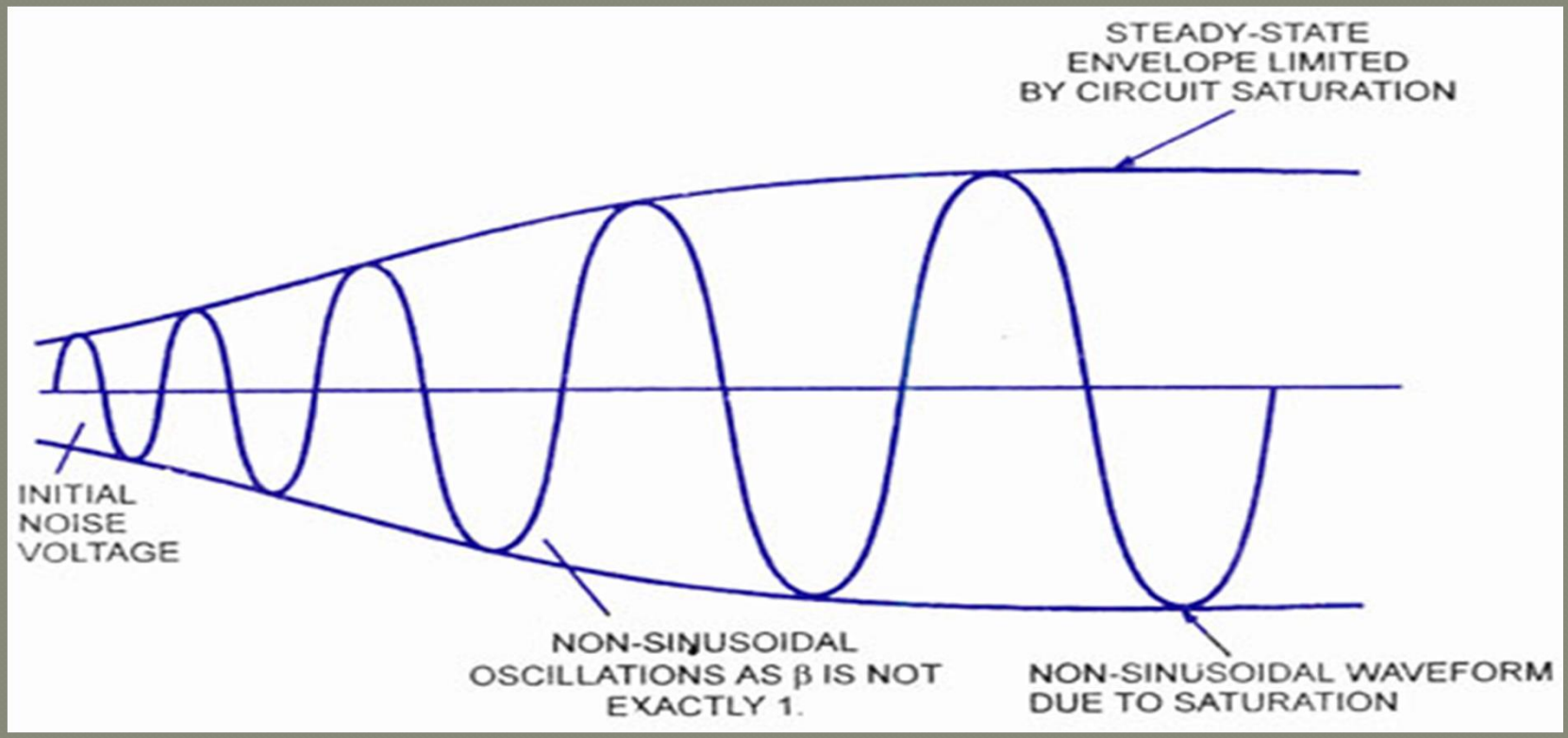
$$V_f = \beta*V_O$$

$$V_f = A*\beta* V_i$$

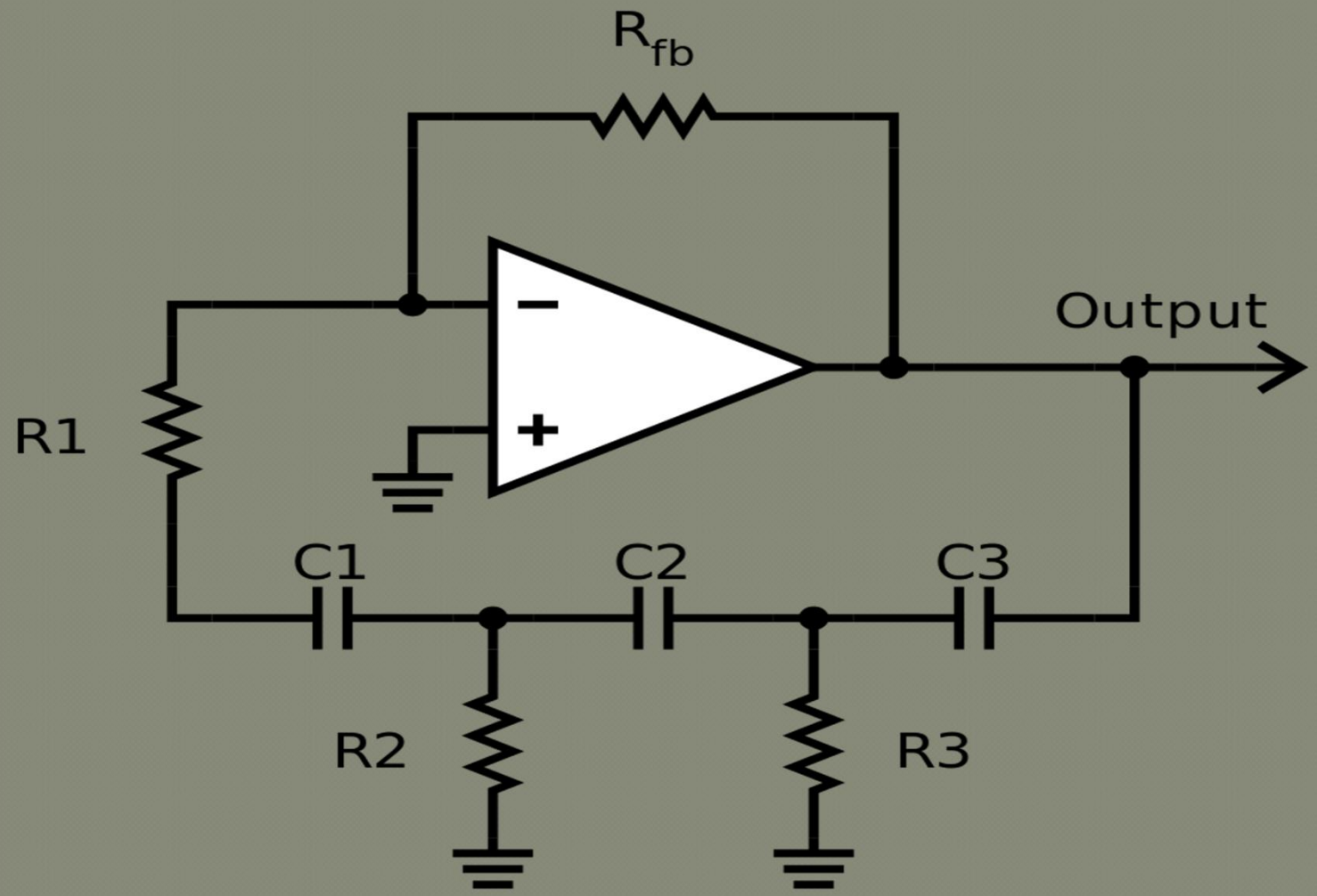
- When the switch is closed and the input voltage $\mathbf{V_i}$ is stopped, the output voltage of feedback circuit $\mathbf{V_f}$ should drive the amplifier producing continuous output.

- For this to happen, $|\beta A| = 1$, so that $\mathbf{V_f = V_i}$.

- This condition is called as ***Barkhausen Criteria***.



Phase Shift Oscillator:



Phase Shift Oscillator:

- An oscillator circuit that follows the basic development of a feedback circuit is the Phase Shift Oscillator.
- RC phase shift oscillator basically consists of an Amplifier and a feedback circuit.
- Feedback circuit consists of a resistor and a capacitor (**RC**) connected in parallel.
- Feedback circuit should produce phase shift of 180^0.
- One RC component produces phase shift of 60^0. So to get180^0 phase shift, we need to use 3 RC components which are connected in series.
- Hence in RC Phase Shift Oscillator circuit, feedback circuit consists of 3 RC components.

- The output of the amplifier is given to feedback network. The output of the feedback circuit drives the amplifier.

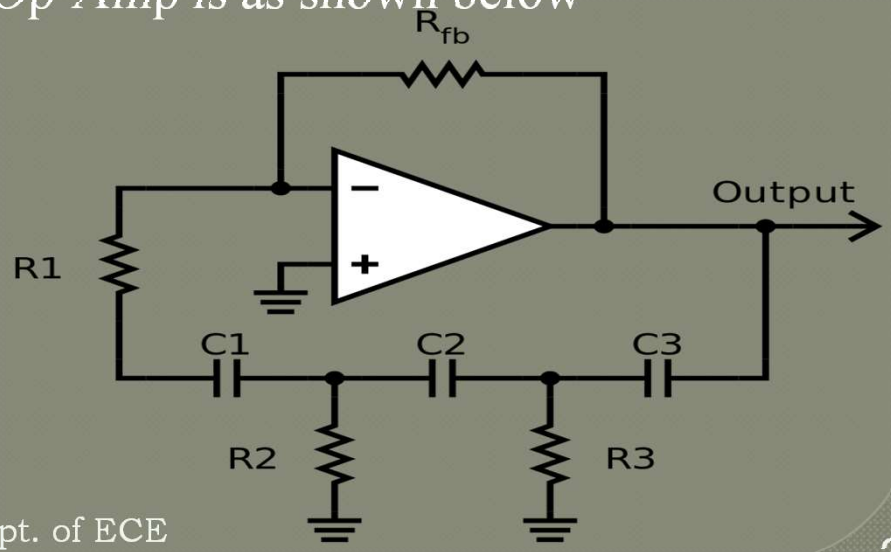
- We find the frequency of the oscillator which is dependent on the values of R and C is given by;

$$f = \frac{1}{2\pi RC\sqrt{6}}$$

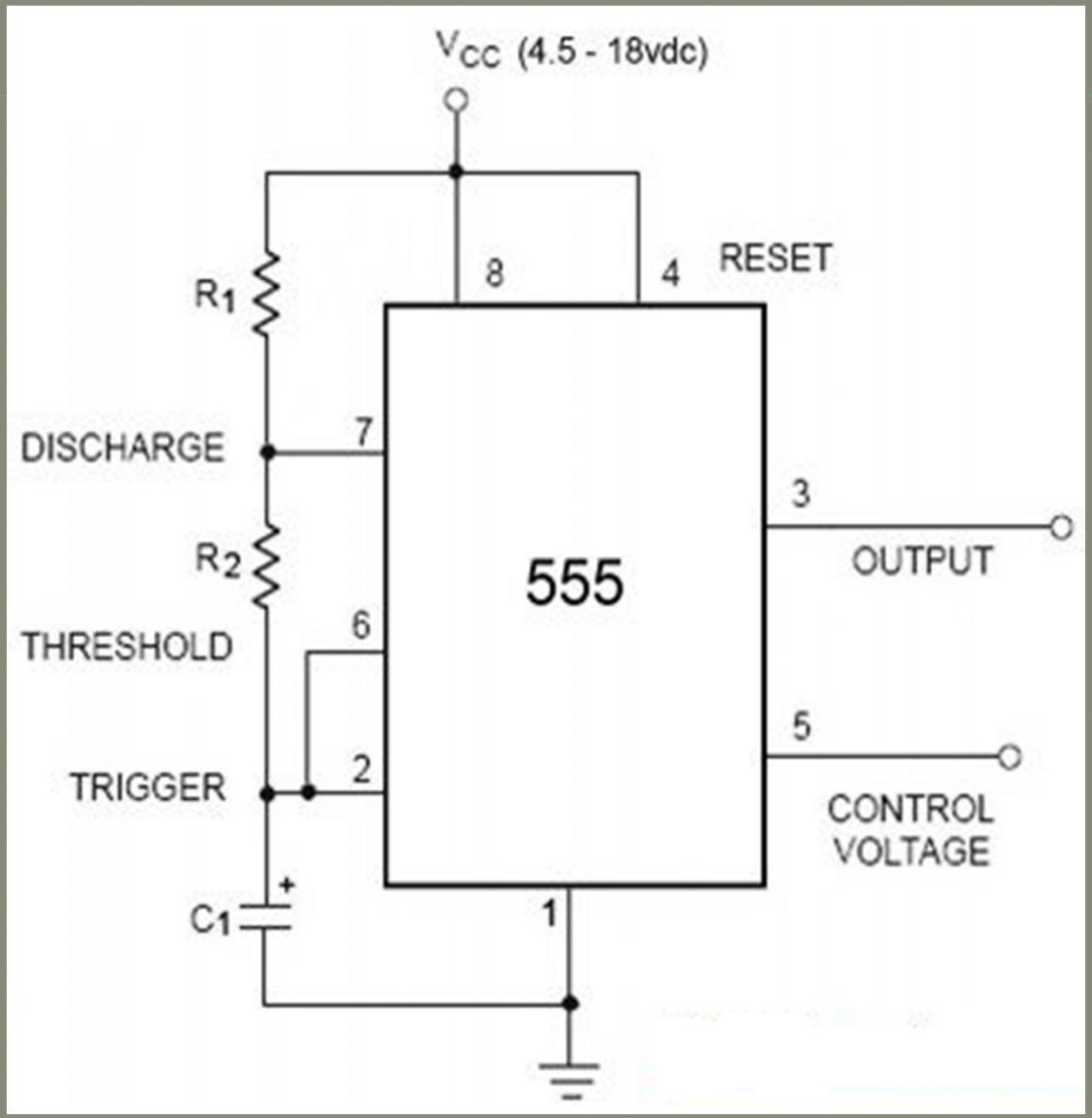
and feedback gain $\boldsymbol{\beta}$ is $\frac{1}{29}$

- For loop gain (βA) to be greater than Unity. Gain of the amplifier stage (A) must be greater than $\frac{1}{\beta}$ or 29. Hence A = 29

- An RC Phase Shift Oscillator with an Op-Amp is as shown below



Astable Operation:



- One of the main applications of 555 timers is as astable multivibrator or clock circuit.

- Figure below shows astable circuit built using two external resistors and a capacitor, which sets the timings in interval of the output.

- The capacitor begins to charge from the DC source V_{CC}, when the voltage of the threshold pin 6tends to increase beyond 2/3 V_{CC}, the comparator 1 saturates and its output triggers the flip-flop and so the output at pin 3 goes low.

- At the same time, the transistor becomes 'On' causing the output at pin 7 to discharge the capacitor through R_2 at time constant $=R_2C$.

- As the capacitor voltage which is the trigger input at pin 2 falls below 1/3 V_{CC}, the comparator 2 output causes the flip-flop to reset, the output at pin 3 becomes high and the transistor goes 'Off'.

- The capacitor begins to charge through R_1 and R_2 at the time constant = $(R_1+R_2)C$. The process then repeats continuously.

- The output waveform and the capacitor charging and discharging are as shown below:
- The charging time and the discharging time is given by T_{High} and T_{Low} which is given by equations:

$$T_{High} = 0.7(R_1+R_2)C$$

$$T_{Low} = 0.7\ R_2C$$

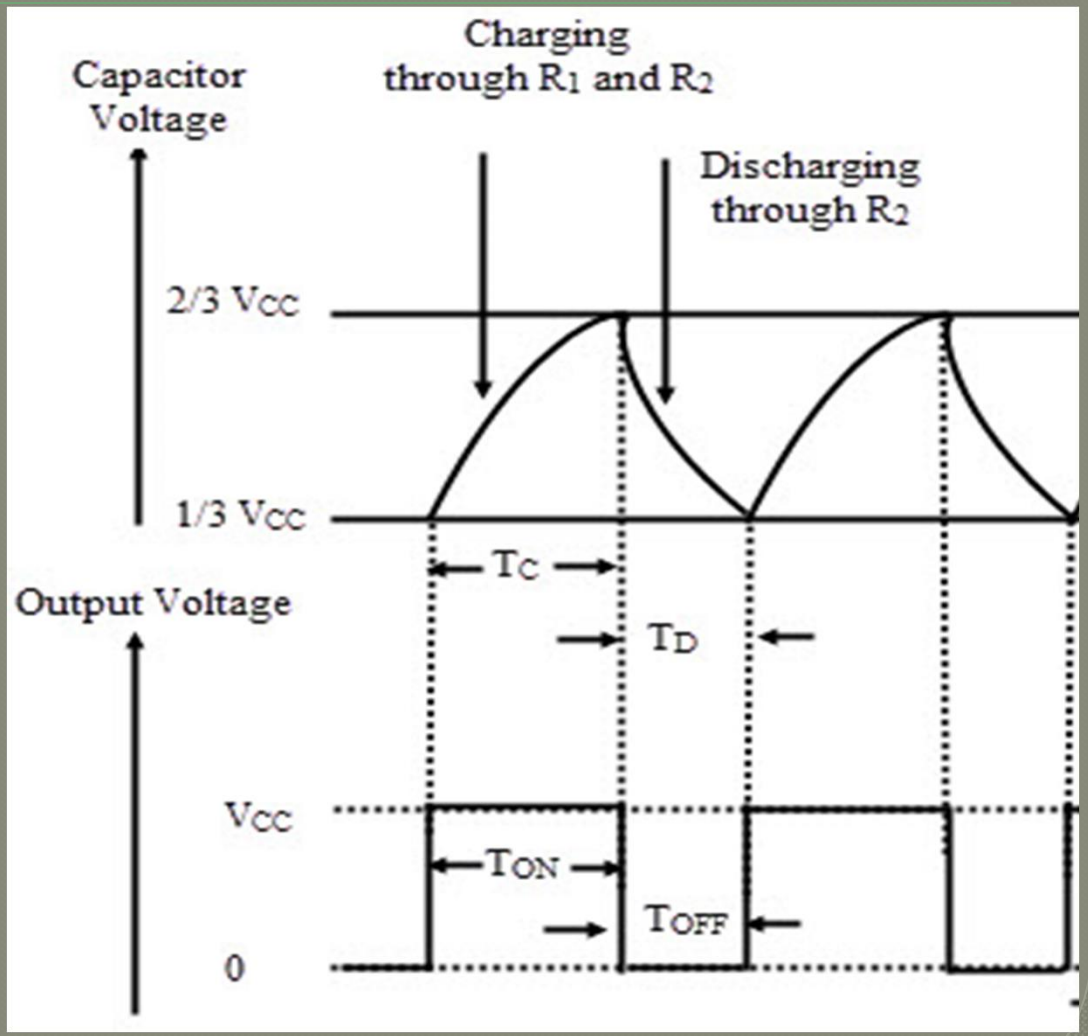
The oscillator period:

$$T = T_{High} + T_{Low}$$

The oscillator frequency:

$$f = \frac{1}{T} = \frac{1.44}{(R_1+2R_2)C}$$

Duty cycle is less than 50%.



THANK YOU

BASIC ELECTRONICS (18ELN13/23)

MODULE 5

DIGITAL ELECTRONICS FUNDAMENTALS

Presented by
Lakshmi D L
Asst. prof., Dept. of ECE
BGSIT, BG Nagara

Difference between Analog Signal and Digital Signal:

COMPARISON PARAMETER	ANALOG SIGNAL	DIGITAL SIGNAL
Basic	An analog signal is a continuous wave that changes over a time period	A digital signal is a discrete wave that carries information in binary form
Representation	An analog signal is represented by a sine wave 	A digital signal is represented by a square waves 
Description	An analog signal is described by the amplitude, period or frequency and phase	A digital signal is described by the bit rate and bit intervals
Range	An analog signal has no fixed range	Digital signal has a finite range i.e. between 0 and 1
Distortion	An analog signal gets more infected to distortion	A digital signal is less infected to distortions
Transmit	An analog signal transmits data in the form of a wave	A digital signal carries data in the binary form
Example	Human Voice, Musical Instrument Sounds	Signals used for transmission in the Computer

NUMBER SYSTEM

- There are 4 number systems of arithmetic that are used in the digital systems:
  - Decimal
  - Binary
  - Hexadecimal
  - Octal

- Number systems are classified based on its "Radix Number" or "Base Number"

- Radix number for:
  - Binary is '2' = ($)_2$
  - Decimal is '10' = ($)_{10}$
  - Hexadecimal is '16' = ($)_{16}$
  - Octal is '8' = ($)_8$

- **Binary Number System:**
- These are represented by **Radix** or **Base 2.**
- These consist of 0's and 1's.
- Binary digits are also called 'Bits'.

- **Decimal Number System:**
- These are represented by Radix or **Base 10**
- It consists of numerals from 0 – 9.

- **Hexadecimal Number System:**
- These are represented by Base or **Radix 16**.
- It consists of numerals from 0 – 15.
- Numerals 10,11,12,13,14,15 are represented by A,B,C,D,E,F respectively called as Alphanumerals.

- **Octal Number system:**
- These are represented by Base or **Radix 8**
- It consists of numerals from 0-7
- The octal system is formed by grouping bits in groups of 3, starting at the binary point.

CONVERSION TABLE

Decimal	Binary	Hexadecimal	Octal
0	0000	0	0
1	0001	1	1
2	0010	2	2
3	0011	3	3
4	0100	4	4
5	0101	5	5
6	0110	6	6
7	0111	7	7
8	1000	8	10
9	1001	9	11
10	1010	A	12
11	1011	B	13
12	1100	C	14
13	1101	D	15
14	1110	E	16
15	1111	F	17

COMPLEMENTS

- **1's complement representation**
- The 1's complement of a binary number is the number that results when all 1's changes to 0's and all 0's changes to 1's.

- **2's complement representation**
- The 2's complement is the binary number that results when 1 is added to the 1's complement.

- 2's complement = 1's complement + 1

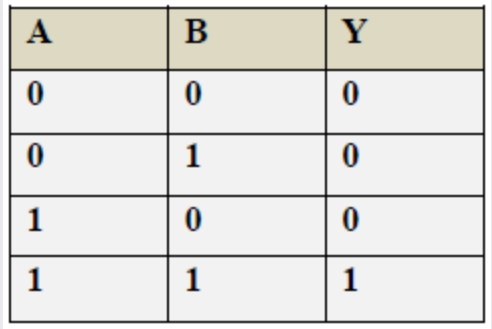
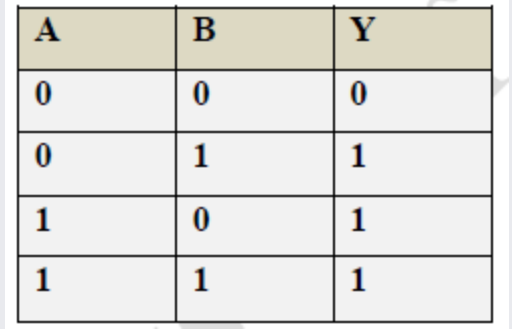
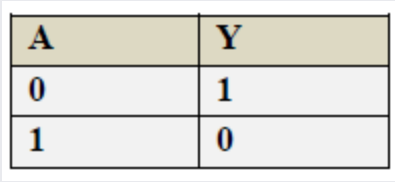
Binary subtraction using 1's complement method:

- A-B is performed using the following steps:
- Take 1's complement of B
- Result= A+1's complement of B
- If carry is generated then the result is positive. Add carry to the result to get the final result.
- If carry is not generated then the result is negative, take 1's complement and assign –ve sign to get the final result.

Binary subtraction using 2's complement method:

- A-B is performed using the following steps:
- Take 2's complement of B
- Result= A+2's complement of B
- If carry is generated then the result is positive. Ignore the carry to get the final result.
- If carry is not generated then the result negative, take 2's complement and assign –ve sign to get the final result.

Boolean Algebra Theorems:

1. AND – Multiplication Symbol (·)	2. OR – Addition Symbol (+)	3. NOT – Complement
Y = A AND B = A · B	Y = A OR B = A + B	Y = NOT (A) = A'
		
In AND operation, the output is 1 only if both A and B are 1; otherwise it is 0	In OR operation, the output is 1 if either A or B or both are 1	In NOT operation, the output is the reverse of input.

Identities of Boolean Algebra

Name	AND form	OR form
Identity law	$1 \cdot A = A$	$0 + A = A$
Null law	$0.A = 0$	$1 + A = 1$
Idempotent law	$A \cdot A = A$	$A + A = A$
Inverse law	$A \cdot A' = 0$	$A + A' = 1$
Commutative law	$A \cdot B = B \cdot A$	$A + B = B + A$
Associative law	$(A \cdot B) \cdot C = A \cdot (B \cdot C)$	$(A + B) + C = A + (B + C)$
Distributive law	$A + BC = (A + B) \cdot (A + C)$	$A(B + C) = AB + AC$
Absorption law	$A \cdot (A + B) = A$	$A + AB = A$
De Morgan's law	$(A \cdot B)' = A' + B'$	$(A + B)' = A'B'$

Digital Circuits:

- Digital circuits are classified into two major categories:

1. **Combinational Circuits and**
2. **Sequential Circuits.**

- Combinational Circuits are the circuits where output depends on the present input only.
- The sequential circuit produces the output on the basis of the both present and previous inputs.

Logic Gates:

- Logic Circuits are the building blocks of digital circuits.
- They are used to create digital circuits and even complex integrated circuits.
- Logic Gates are classified as **Basic Gates** and **Universal Gates**.
- Basic gates are **AND, OR** and **NOT**.
- Universal gates are **NAND, NOR**.

Logic Gates

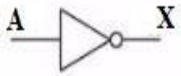
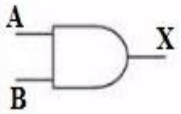
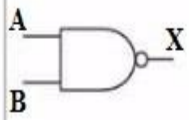
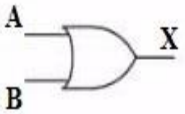
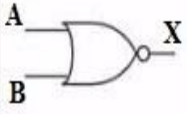
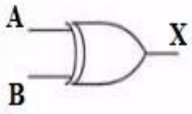
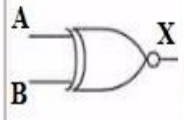
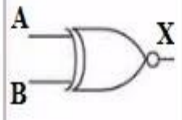
NOT	AND	NAND	OR	NOR	XOR	XNOR	BUFFER
$\overline{A}$	AB	$\overline{AB}$	$A+B$	$\overline{A+B}$	$A \oplus B$	$\overline{A \oplus B}$	A
							
A X 0 1 1 0	A B X 0 0 0 0 1 0 1 0 0 1 1 1	A B X 0 0 1 0 1 1 1 0 1 1 1 0	A B X 0 0 0 0 1 1 1 0 1 1 1 1	A B X 0 0 1 0 1 0 1 0 0 1 1 0	A B X 0 0 0 0 1 1 1 0 1 1 1 0	A B X 0 0 1 0 1 0 1 0 0 1 1 1	A B X 0 0 1 0 1 0 1 0 0 1 1 1
a	b	c	d	e	f	g	g

Fig: Logic gates Symbol and Truth table

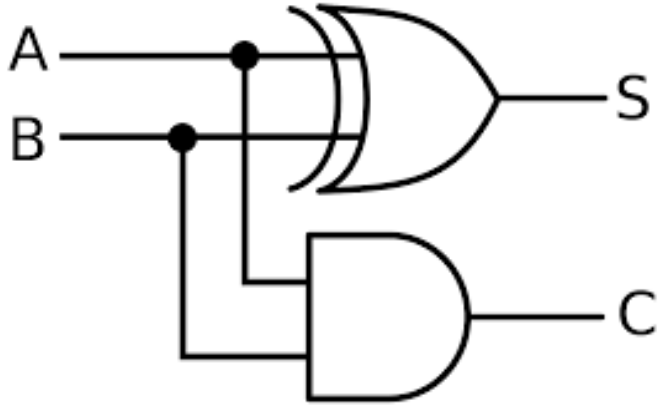
ADDERS:

- Adders are the logical circuit which adds two or more binary bits whose outputs are **Sum** and **Carry**.

- It is classified into two types:
  1. **Half Adder**
  2. **Full Adder**

HALF ADDER:

- Half adder is an example of a simple functional circuit built from two logic gates.
- The half adder adds two one-bit binary numbers (A, B).
- The output is the SUM (S) of the two input bits and the Carry (C).
- The below figure shows the schematic of half adder circuit.

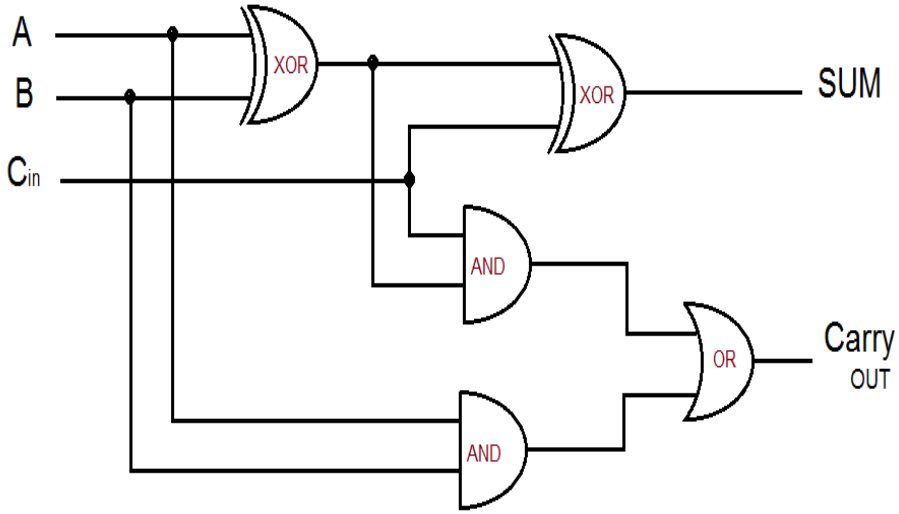


INPUT		OUTPUT	
A	B	SUM(S)	CARRY(C)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

$$S = \bar{A}B + A\bar{B} = A \oplus B$$

$$C = AB$$

FULL ADDER:



- Full adder adds three one-bi binary numbers (A, B, Cin) and outputs two one-bit binary numbers, SUM (S) and Carry (Co).

$$S = \bar{A}\bar{B}C_{in} + \bar{A}B\overline{C_{in}} + A\bar{B}\overline{C_{in}} + ABC_{in}$$

$$S = A \oplus B \oplus C_{in}$$

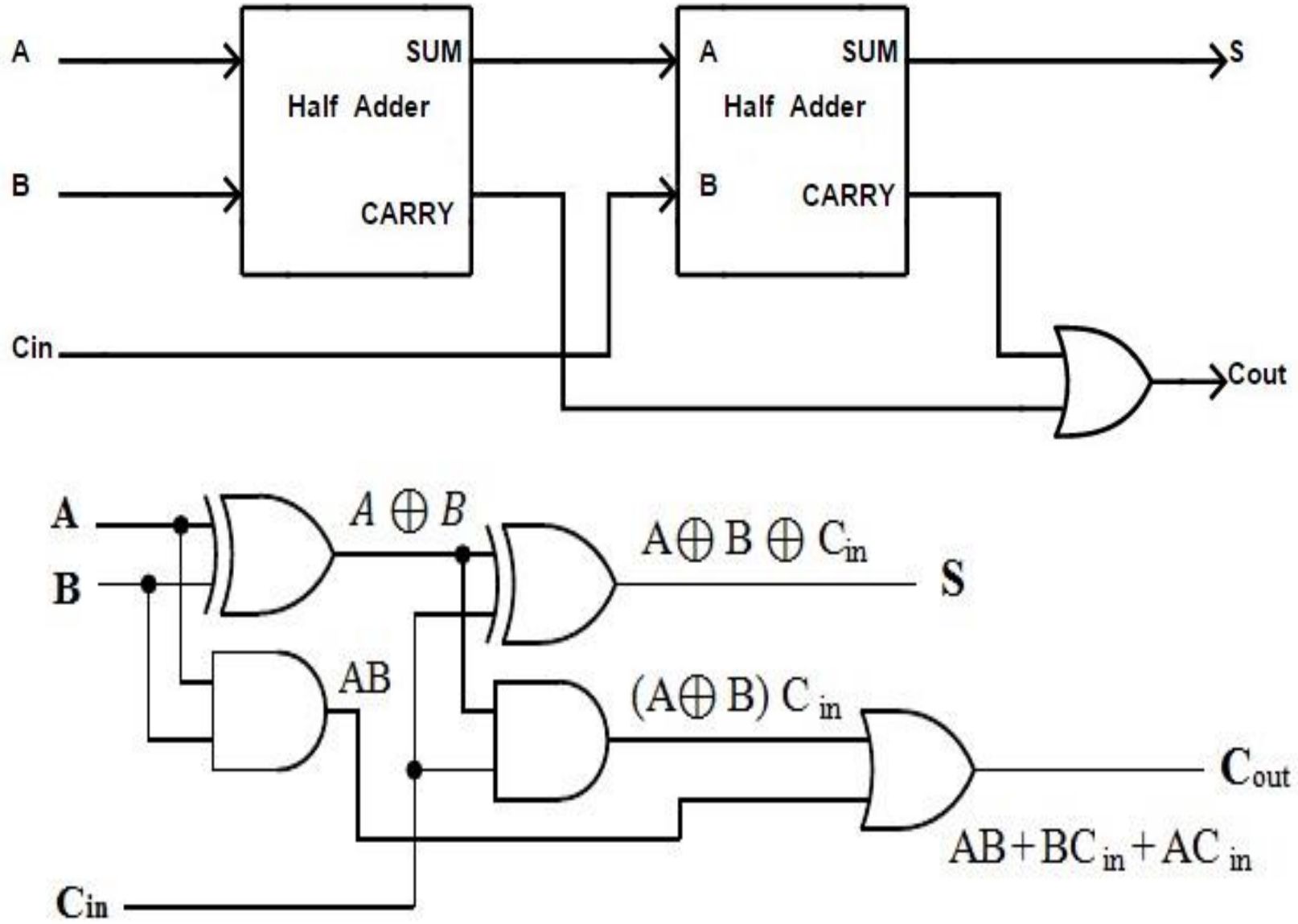
$$C_{out} = \bar{A}BC_{in} + A\bar{B}C_{in} + AB\overline{C_{in}} + ABC_{in}$$

$$C_{out} = AB + BC_{in} + AC_{in}$$

INPUT			OUTPUT	
A	B	C_{in}	SUM(S)	CARRY(C_{out})
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Implementation of Full adder Using Two Half Adders:

- Full adder can be realized using two half adders.
- The Half Adder1 Sum output is given as one of the input to the Half Adder2 with C_{in} as another input which gives the SUM of the full adder.
- The Half Adder1 carry is given as one of the input to the OR gate with carry of Half Adder2 which produces the Carry Out of full adder.



Full adder using 2 Half adders

Multiplexers:

- The objective of a multiplexer is to select one signal from a group of 2^n inputs to be an output.
- In 8:1 Multiplexer, Lines **D0, D2, D3, D4, D5, D6, and D7** are the data input lines and Y is the output line.
- Lines **A, B and C** are called the **select lines**. They are three bit binary numbers which are used to choose one of the D input lines to be output on the line Y.
- Suppose if D5 is to be on output line, i.e. Y=D5, then the corresponding select inputs are 5 = 101 or AB'C.
- The output Y will be the sum of all the $8(2^3)$ inputs.

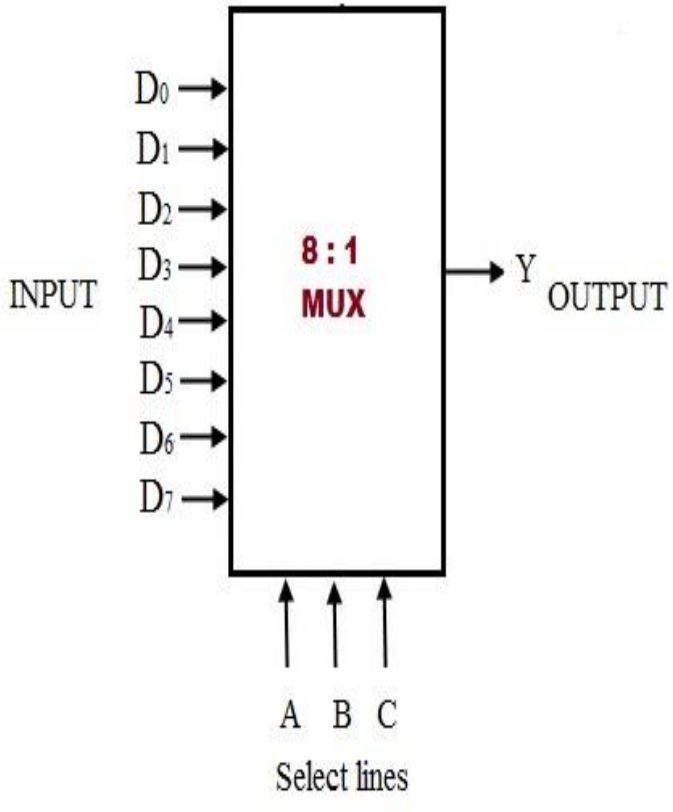


Fig. 8:1 Multiplexer

Select data Inputs			Out put
A	B	C	Y
0	0	0	D_0
0	0	I	D_I
0	I	0	D_2
0	I	I	D_3
I	0	0	D_4
I	0	I	D_5
I	I	0	D_6
I	I	I	D_7

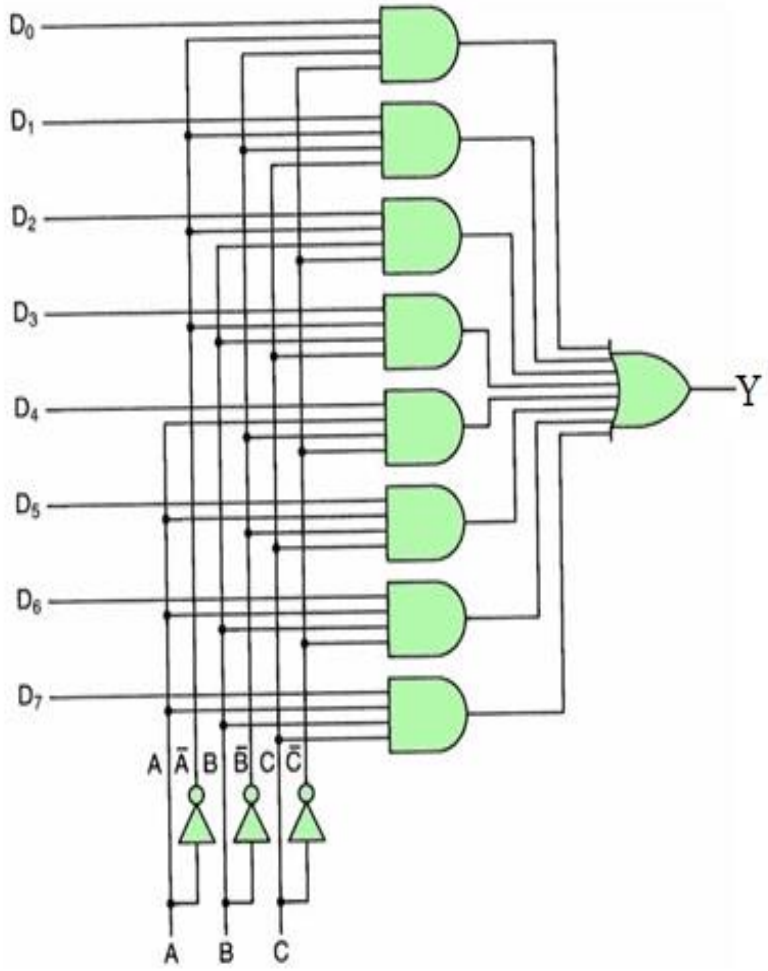


Fig. Gate level diagram of 8:1 Multiplexer

Decoders:

- The objective of the decoder is to decode an n-bit binary number, producing a signal on one of the 2n output lines.
- The same circuit is used as de-multiplexers.
- To produce D6 as output, then inputs A=1, B=1, and C=0 or ABC’

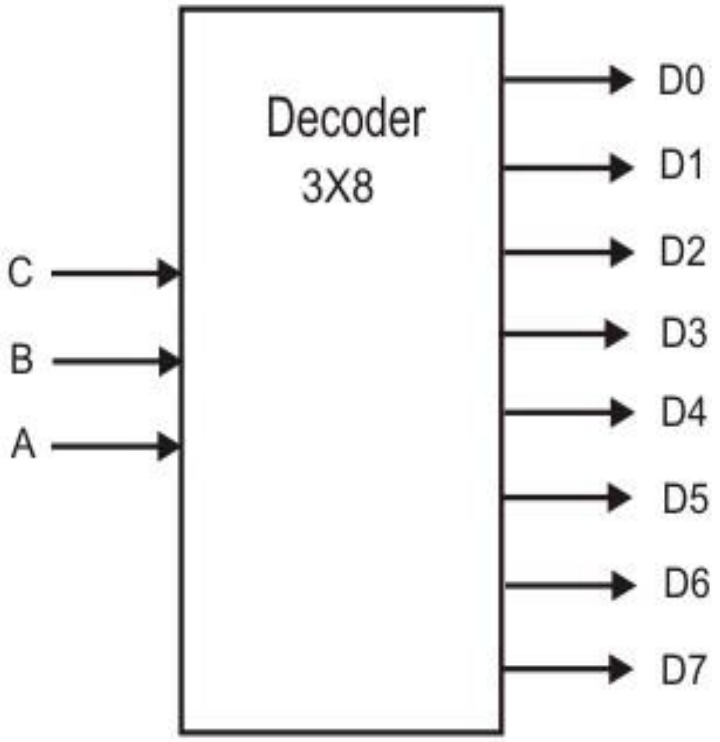


Fig. 3:8 decoder

INPUT			OUTPUT							
A	B	C	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

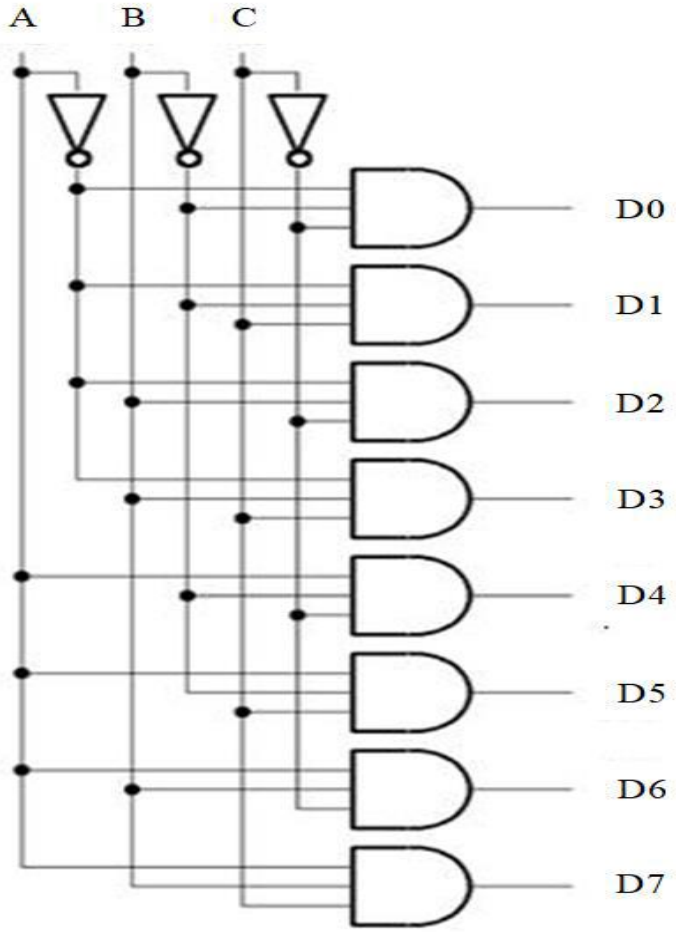
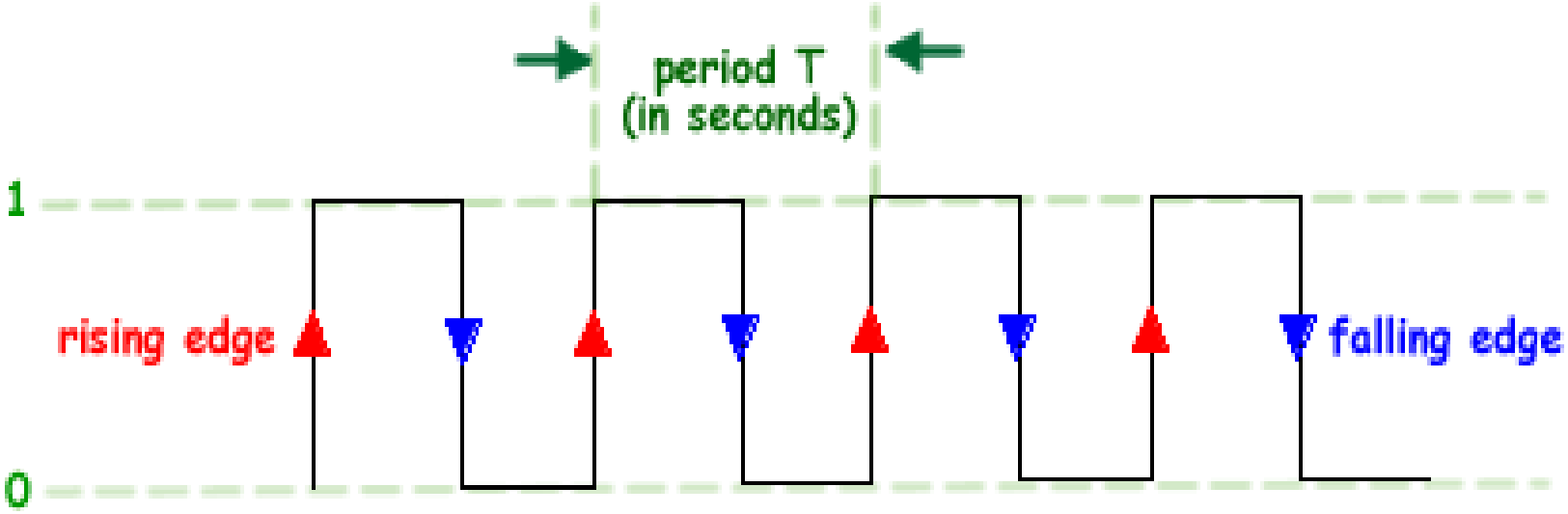


Fig. Gate level diagram of 3:8 de-multiplexers

Flip-Flop:

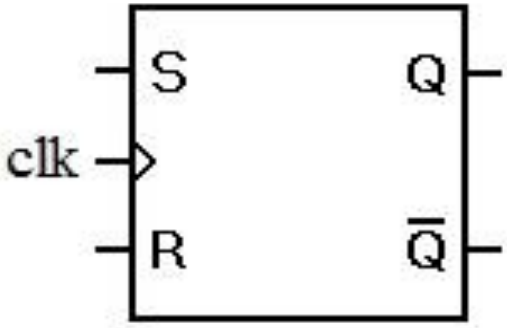
- Flip flop is an electronic circuit that has two stable states and can be used to store One bit data.
- Flip flops are the basic memory elements of the sequential circuits.
- There are different types of Flip-Flops:
- 1. SR Flip Flop
- 2. D Flip Flop
- 3. T Flip Flop
- 4. JK Flip Flop

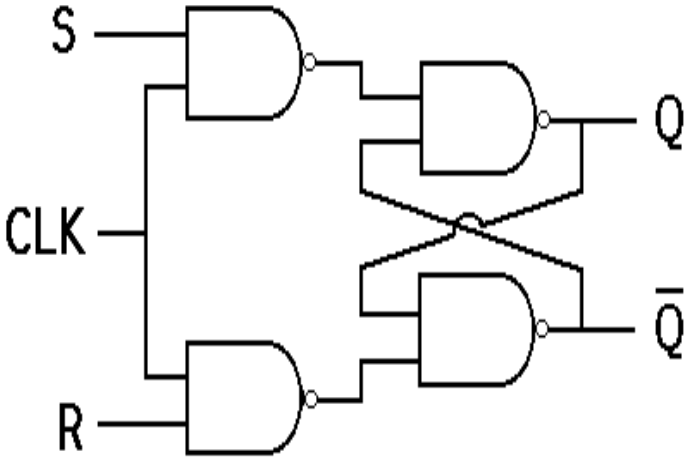
- **CLOCK**: A clock is used to synchronize changes in the contents of memory element. A clock is a signal which oscillates between 0 and 1.



- When Clk=0, the output of both AND gate is 0. So Q cannot change. The latch is non-operational.
- When Clk=1, the output of upper NAND gate is 1·S=S and output of lower NAND gate is 1·R=R, the latch is now operational. (fig. clocked SR Flip flop)

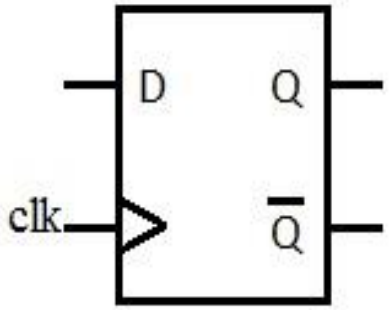
1. Clocked SR (Set-Reset) Flip Flop:

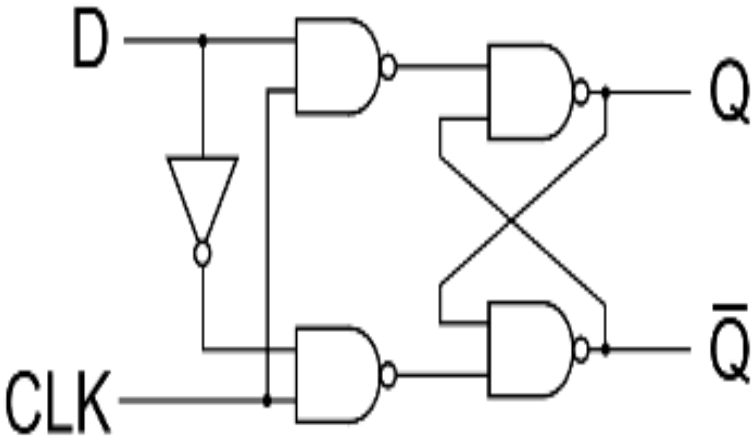




Clk	S	R	Q	Q'	STATE
0	X	X	Q	Q'	**Previous State**
1	0	0	Q	Q'	**Previous State**
1	0	1	0	1	**Reset**
1	1	0	1	0	**Set**
1	1	1	1	1^*	**Forbidden**

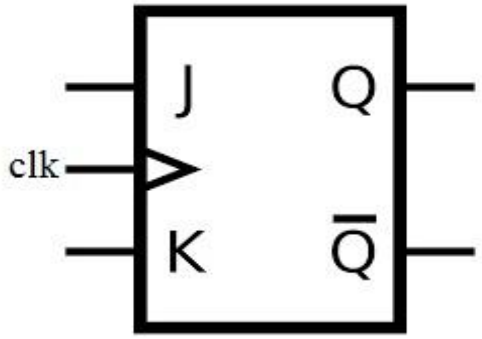
2. Clocked D Flip Flop:

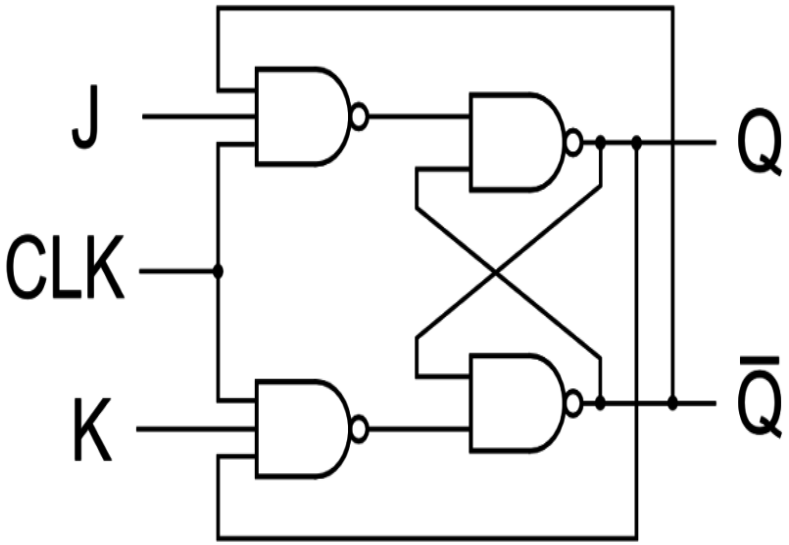




Clk	D	Q
0	X	**Previous State**
1	0	**0**
1	1	**1**

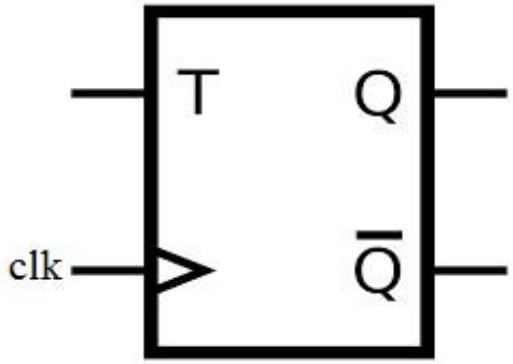
3. Clocked JK Flip Flop:

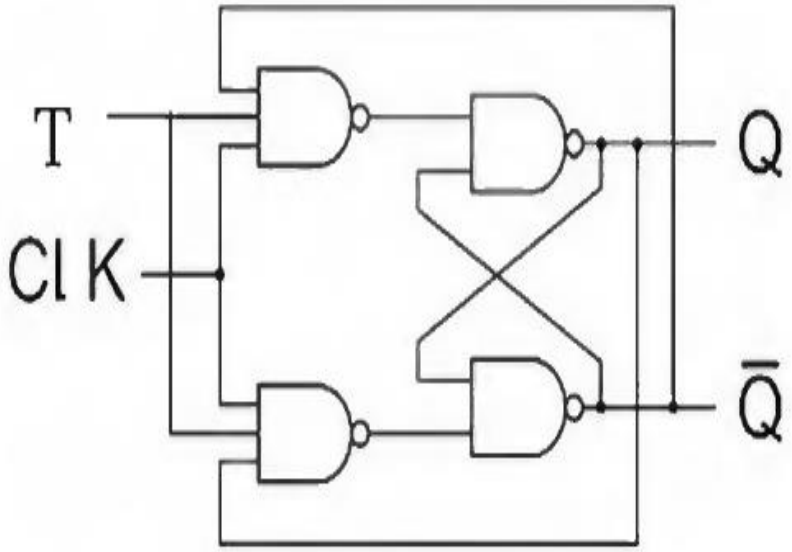




Clk	J	K	Q	Q'	state
0	X	X	Q	Q'	**Previous state**
1	0	0	Q	Q'	**No change**
1	0	1	0	1	**Reset**
1	1	0	1	0	**Set**
1	1	1	Q'	Q	**Toggle**

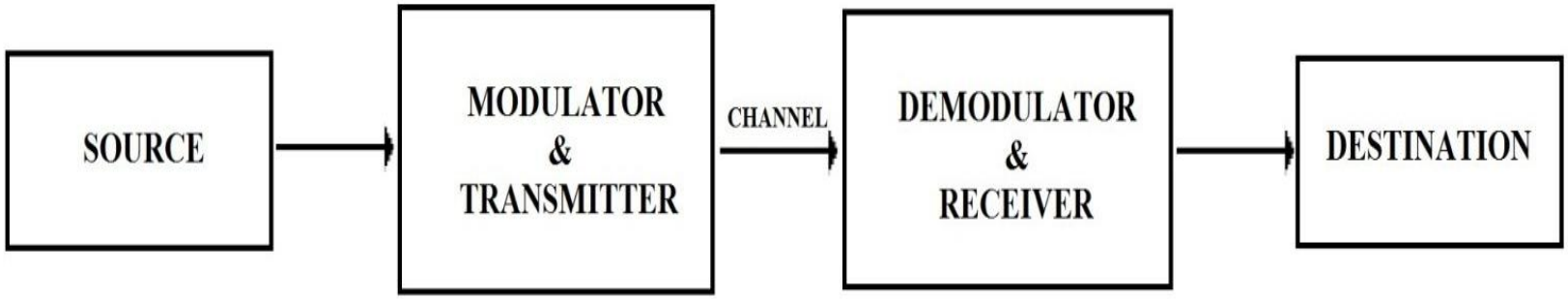
4. Clocked T Flip Flop:





clk	T	Q
0	X	Q (Previous state)
1	0	Q (Previous state)
1	1	Q'

ELEMENTS OF COMMUNICATION SYSTEMS:



- **Information Source:**
- It generates the message or the information to be transmitted. This message signals are non-electrical in nature.
- Eg: Text, Voice, Picture, Video etc.

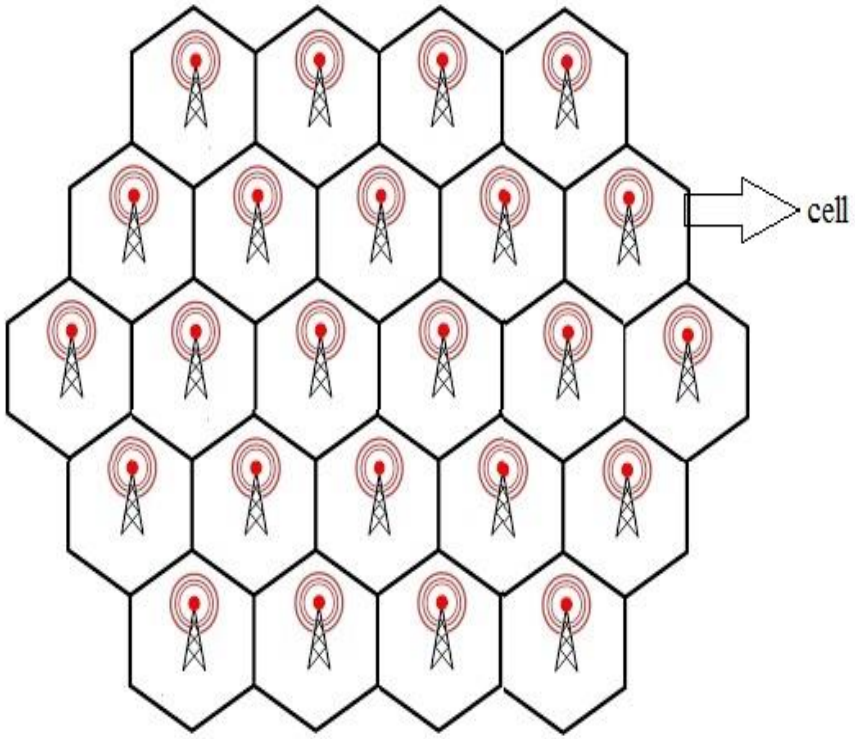
- **Modulator and Transmitter:**
- Modulator is an electronic device, which converts the non-electrical signal into electrical signal suitable for transmission over a channel.
- It consists of Transducer, Encoder, Amplifier, and Modulator to make the signal suitable for transmission.

- **Channel:**
- Channel is a medium through which the electrical signal is transmitted from one place to another.
- Communication channel can be wired (Co-axial cable, OFC, Twisted pair cable) or wireless.

- **Noise Source:**
- Noise is an unwanted signal that gets added to the message signal during transmission over the channel.
- Noise may be natural or man-made.

- **Receiver and Demodulator:**
- It is a collection of electronic circuit designed to convert the modulated signals back to the original information.
- It consists of transducer, decoder, amplifier, demodulator to get original signal from electrical signal and received at the destination.

PRINCIPLE OF OPERATIONS OF MOBILE PHONE:



- A cellular/mobile system provides standard telephone operation by full-duplex two-way radio at remote locations.
- It provides a wireless connection to the **Public Switched Telephone Network (PSTN)** from any user location within the radio range of the system.
- The basic concept behind the cellular radio system is that rather than serving a given geographical area within a single transmitter and receiver, the system divides the service area into many small areas known as **Cells**.

The cells area is an ideal Hexagon. But in reality they will have circular or other geometrical shapes.

- A basic cellular system consists of mobile stations, base stations and a Mobile Switching Center (MSC), which is also known as Mobile Telephone Switching Office (MTSO).
- These MTSO controls the cells and provides the interface between each cell and the main telephone office.
- Each mobile station consists of a **transceiver**, an antenna and control circuit.
- The base station consists of several transmitters and receivers which simultaneously handle full-duplex communication.
- The base station serves as a bridge between all mobile users in the cell and connects the simultaneous mobile call via telephone lines or microwave link to the MSC.
- The MSC co-ordinates the activities of all the base stations and connects the entire cellular system to the PSTN.
- Most cellular system provides a service known as **roaming**.

CELLULAR TELEPHONE UNIT:

- Figure shows the block diagram of a cellular mobile radio unit. The unit consists of 5 major blocks.

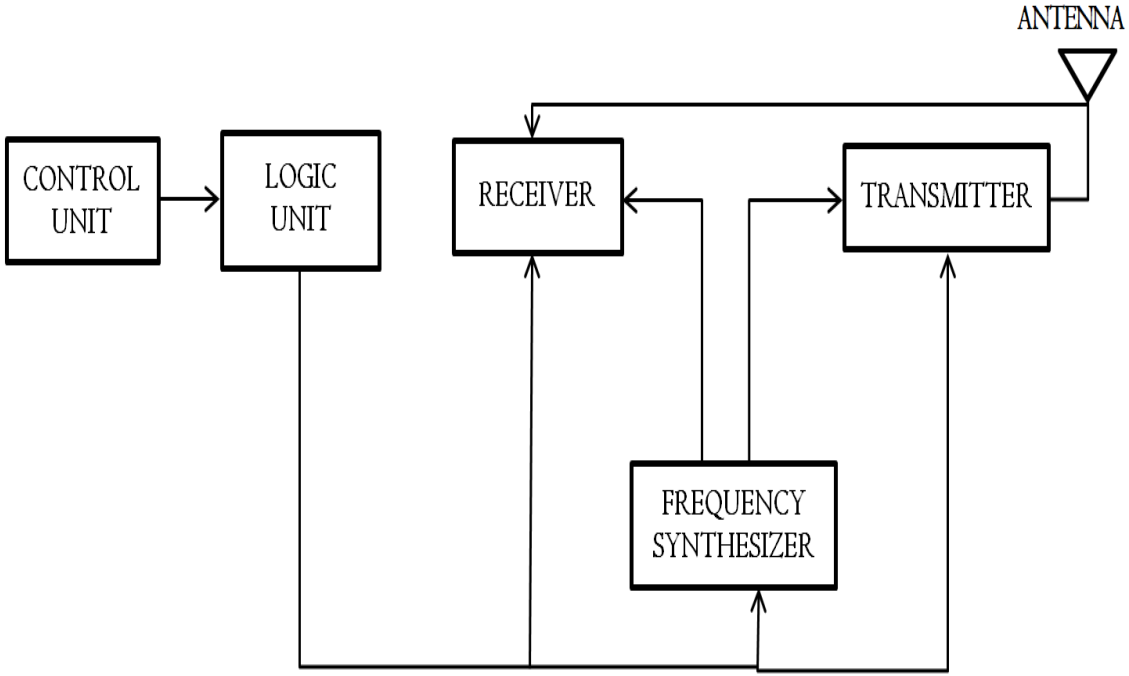
1. Control unit

2. Logic unit

3. Receiver

4. Frequency Synthesizer

5. Transmitter



- **Control Unit:**

- The control unit is a set of speakers, microphone with touch tone dialing facility and it stores the memory like numbers and dialing features.

- **Logic Unit:**

- Logic unit is micro-processor controlled master control circuit for cellular radio.
- It basically controls the complete operation of MTSO and mobile unit.

- **Receiver:**

- Receiver consists of RF amplifier, FM demodulator and filters.
- An RF amplifier boosts the level of received cell site signal.
- Received signal is monitoring by MTSO.
- If the signal is weak in the present cell, then the mobile unit is shifted to other site where the signal is strong.

- **Frequency Synthesizer:**

- It is used to generate various signals required for transmitter and receiver.
- When a mobile unit initiates a call, MTSO identifies the user and assigns a frequency Channel which is not used by any other mobile in the cell.
- MTSO sends a unique code for setting channel frequencies.

- **Transmitter:**

- It is a low power FM transmitter operating in a frequency range of 825 to 845 MHz.
- There is a 66.63MHZ transmitting channel and the Transmitter produces a deviation of 12kHz.
- The modulated output is translated up to final transmitter frequency with the help of a mixer, whose second input comes from the frequency synthesizer.
- The basic feature of high power translator is that output is controllable by the cell site and MTSO.

THANK YOU